Siliconix

APPLICATION NOTE

Junction FETs In Active Double-Balanced Mixers

Ed Oxner

June, 1973

Introduction

Dynamic range is probably the most important consideration in modern receiver design. An earlier Siliconix Application Note (1) provided a comparison between the harmonic distortion characteristics of a simple mixer, a single-balanced mixer, and a double-balanced mixer (Table I). The comparison clearly shows those performance characteristics of the double-balanced mixer which have made it the most popular of all mixer types. Among these attributes are greatly improved interport isolation and a significant degree of rejection of local oscillator carrier amplitude modulation.

When used in double-balanced mixers, however, passive devices such as Schottky-barrier (hot carrier) diodes have certain fundamental shortcomings, such as high conversion loss and high local oscillator drive requirements. Thus the active balanced mixer which employs field-effect transistors is a welcome innovation: conversion gain and improved intermodulation distortion characteristics alone place the FET double-balanced mixer far ahead of its passive counterparts. The high saturation levels possible with modest local oscillator power make such a mixer useful for mixing both small and large signals.

In the past, double-balanced mixers built around MOS FET technology have been considered. (2,3,4) Heretofore, the MOS FETs have been used solely as switching devices, requiring no external DC power. As a result, all MOS FET mixers to date have exhibited high conversion loss, and require considerable local oscillator drive power.

TABLE I

Characteristic	MIXER TYPE		
	Single-Ended	Single Balanced	Double Balanced
Bandwidth	Several decades possible	Decade	Decade
Relative IM Density	1.0	0.5	0.25
Interport Isolation	Little	10-20 dB	> 30 dB
Relative L.O. Power	0 dB	+3 dB	+6 dB

x

Copyright 1973 Siliconix Inc.

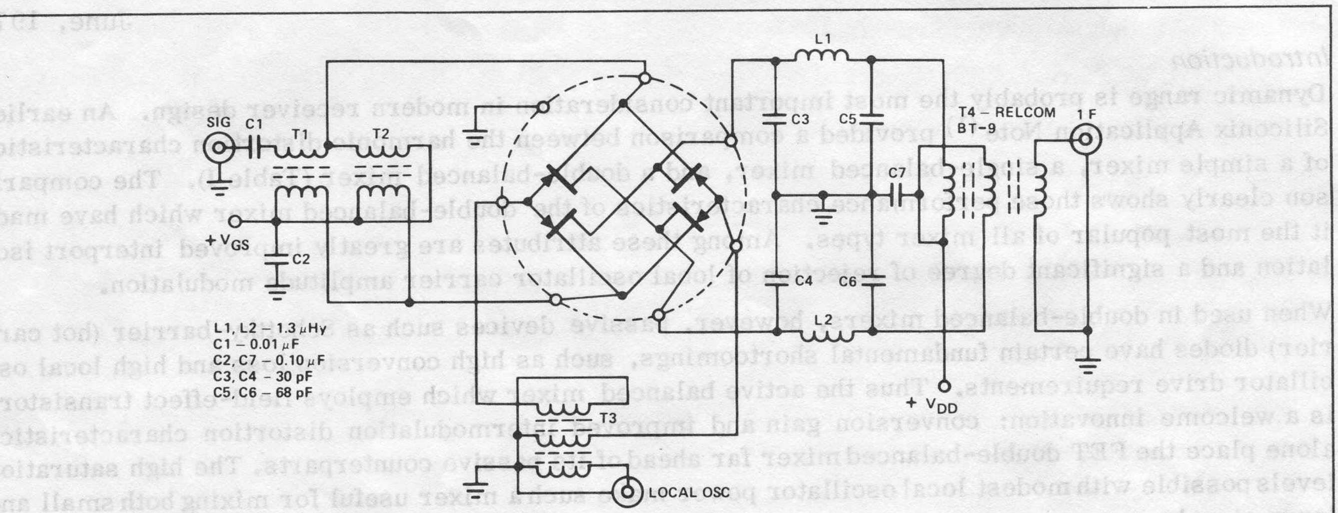
First Order Double-Balanced Mixer Theory

In either single or double-balanced mixer design, the prime requirement is that when the mixer is excited by the local oscillator carrier, the circuit must be capable of rejecting the amplitude-modulated wave which exists about the L.O. Also, the mixer must reject any AM signal entering from the local oscillator port. (This signal rejection is usually known as AM local oscillator noise cancellation).

A second requirement for balanced mixers is the establishment of interport isolation between the signal, local oscillator, and IF ports. A third desirable characteristic is the reduction of intermodulation distortion products.

Careful attention to design of double-balanced mixers will satisfy the foregoing criteria.

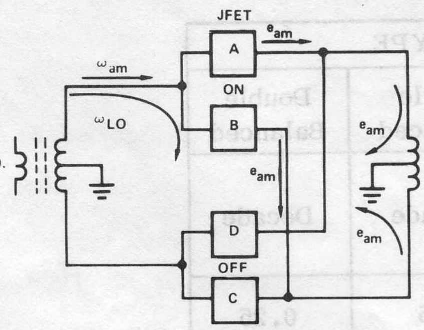
The schematic of a prototype double-balanced mixer (Figure 1) employs four high-performance junction FETs chosen for closely matched characteristics. (The significance of the quad-FET configuration will be dealt with later in this presentation).



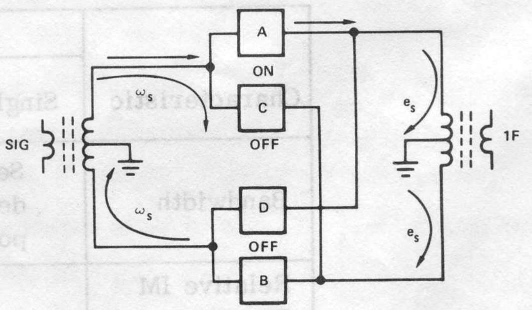
(Figure 1)

Double-Balanced Mixer

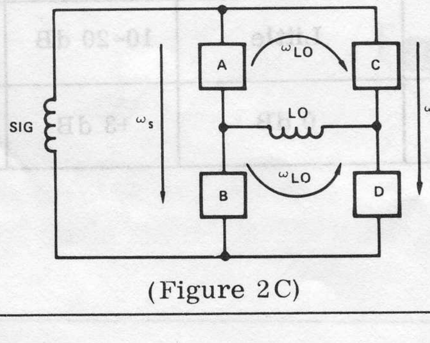
If the schematic in Figure 1 is reduced to show only the local oscillator circuit (Figure 2A), the rejection mechanism of AM signals, either on the L.O. carrier or entering through the local oscillator port, is readily understood.



(Figure 2A)



(Figure 2B)



(Figure 2C)

Likewise, the equivalent circuit in Figure 2B demonstrates how the signal is enhanced at the IF output. Both local oscillator AM cancellation, as well as signal enhancement, are dependent upon the precise balance of the IF transformer, as well as on the match of the four FETs which make up the quad network. In Figure 2C, the schematic has been rearranged to show both the local oscillator and the signal input transformers; the mechanics of interport isolation may be easily visualized. Signal excitation provides an equipotential at the junctions of the local oscillator transformer and FET pairs AB and CD; in the same manner, excitation of the local oscillator produces an equipotential balance at the junctions of the signal transformer and FET pairs AC and BD.

Harmonic distortion products are reduced by the balance between the signal and local oscillator (inputs) and the IF (output), where even-integer harmonics of the signal and local oscillator frequencies are effectively cancelled. A sixth-order summary of such products in both single- and double-balanced mixers is shown in Table II. Note how the relative densities agree with Table I. The effects of harmonic distortion can be reduced by a judicious selection of the IF passband response. [5,6] Third-order IMD (Intermodulation Distortion) products are reduced by virtue of the characteristics of junction FETs, which approximate a square-law response. Care must be taken in FET operation, however, to avoid driving the device into forward conductance by the application of too much local oscillator power.

TABLE II

COMPARISON OF MODULATION PRODUCTS IN SINGLE AND DOUBLE BALANCED MIXERS TO 6th ORDER

Single-Balanced	Double-Balanced
f_s	
$3f_s$	
$5f_s$	
$f_o \pm f_s$	$f_o \pm f_s$
$f_o \pm 3f_s$	$f_o \pm 3f_s$
$f_o \pm 5f_s$	$f_o \pm 5f_s$
$2f_o \pm f_s$	
$2f_o \pm 3f_s$	
$3f_o \pm f_s$	$3f_o \pm f_s$
$3f_o \pm 3f_s$	$3f_o \pm 3f_s$
$4f_o \pm f_s$	
$5f_o \pm f_s$	$5f_o \pm f_s$

Harmonic Distortion, Intermodulation Products, and Cross-Modulation

Spurious output signals in mixers fall into three categories:

(1) Spurious mixer products derived from harmonic mixing of the signal and local oscillator frequencies;

(2) Two-tone, odd-order intermodulation products;

(3) "Chirping" which arises from undesired mixing frequencies falling in the IF passband.

The harmonics of a single-signal frequency, when mixed with the harmonics of the local oscillator, produce spurious outputs which are level-dependent on the signal amplitude. These products are greatly reduced by the double-balanced mixer, where the even harmonics are effectively cancelled; when FETs are used, the Taylor-series power expansion falls quickly to zero above the second order.

However, modulation products of a similar nature will arise if the broadband down-converting mixer is not preceded by signal preselection, because of the mixer's equal response to the "image" frequency. Here, perfectly valid signals will mix with the local oscillator producing interfering i-f signals whose only difference, when compared to the desired i-f signal, is that it moves counter to the desired i-f signal when the local oscillator is shifted.

Two-tone, odd-order IM products differ markedly from other spurious signals. This form of harmonic distortion consists of interactions between two or more input signals and their respective harmonics. In turn, these products are mixed with the fundamental and harmonics of the local oscillator, generating spurious products which may fall within the IF passband, on or very near to the desired signal.

Cross-modulation in the active JFET balanced mixer does not pose a serious problem, so long as the signal input is maintained at a high conductance, which will occur with source injection. Cross-modulation is very dependent on and directly related to the impedance across which the signal is impressed. In the active JFET double-balanced mixer this impedance is very low, typically 35 Ω. Consequently, the effects of cross-modulation may be disregarded.

In the mixing process of any active device, the value of the FET drain current may be derived from a knowledge of the transconductance of the device, and the impressed signal voltage, e_g. This is obtained from the Taylor-series power expansion:

$$i_d = g_m e_g + \frac{1}{2!} \frac{\partial g_m}{\partial V_G} e_g^2 + \frac{1}{3!} \frac{\partial^2 g_m}{\partial V_G^2} e_g^3 + \ldots \frac{1}{n!} \frac{\partial^{n-1} g_m}{\partial V_G^{n-1}} e_g^n \qquad (1)$$

which can be broken down into:

TERM	OUTPUT	TRANSFER CHARACTERISTIC
$g_m e_g$	F1, F2	Linear
$\frac{1}{2!} \frac{\partial g_m}{\partial V_G} e_g^2$	2F1, 2F2 F1 ± F2	Second-order square-law
$\frac{1}{3!} \frac{\partial^2 g_m}{\partial V_G^2} e_g^3$	3F1, 3F2 2F1 ± F2 2F2 ± F1	Third order

In FET theory, the second and higher-order derivatives of g_m are absent, and the device thus offers a considerable reduction of both intermodulation products and higher-order harmonics. In the double-balanced mixer, where F1 ± F2 is the desired result, it is well to manipulate mixer design and bias conditions to render $\frac{\partial g_m}{\partial V_G}$ as large as possible, simultaneously reducing all other terms.

Criteria For FET Selection

In balanced mixers using FETs, conversion efficiency of the devices is determined by conversion transconductance, g_c, which in turn is directly related to such FET operating parameters as zero-bias drain current, I_{DSS}, and pinch-off voltage, V_P.

It can be shown that[7]

$$\frac{I_{DSS}}{V_P^2}\left|V_2\right| \approx \frac{g_{fso}}{2V_P}\left|V_2\right| \tag{2}$$

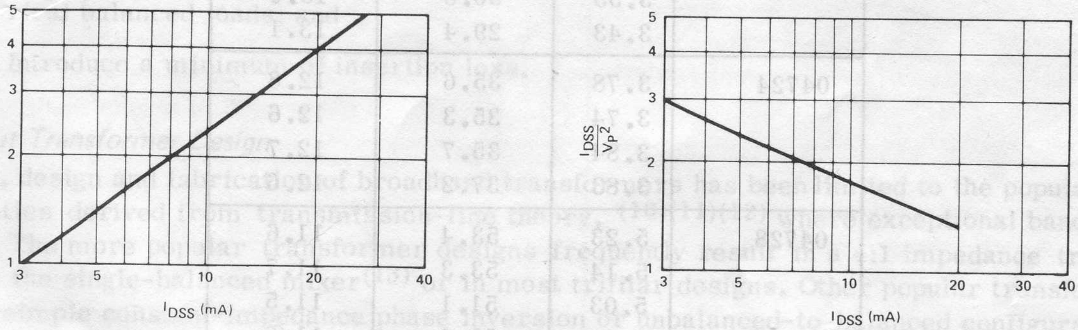
where V_2 is the time-varying local oscillator voltage. To maintain operation in the square-law region

$$V_2\,(\text{peak}) \leq \frac{V_P}{2} \tag{3}$$

where now, under optimum performance conditions, gives

$$g_c \approx \frac{g_{fso}}{2V_P}\,\frac{V_P}{2} = \frac{g_{fso}}{4} \tag{4}$$

For the highest level of conversion transconductance, it would appear initially that for any given FET geometry, units with high I_{DSS} are to be preferred. But since I_{DSS} and V_P are related, a performance tradeoff is necessary. Figure 3 shows that when I_{DSS} is increased conversion transconductance is actually decreased; however, an increased value of I_{DSS} provides increased dynamic range. Since balanced mixer design involves many tradeoffs for best performance, this I_{DSS} vs V_P problem is generally inconsequential.



(Figure 3)
Relationship of I_{DSS} and V_P

For best performance in the single-balanced mixer[8], matched FET pairs were used. A 10% match in pinchoff voltage, V_P, saturated drain current, I_{DSS}, and forward transconductance was sufficient; a wide selection of junction FET pairs is available for single-balanced mixer applications. However, in a double-balanced mixer using a ring-style (quad) demodulator, the match must be extended to four discrete devices. Although high forward transconductance remains desirable, the selection of FETs becomes sharply limited for most users.

Early in the development of the prototype double-balanced mixer, evaluation was made of the potential effect of physical FET packaging on mixer performance. Four selected discrete JFETs were arranged in a matrix which was electrically and schematically identical to the circuit shown in Figure 1. At the same time, four FET chips were mounted in a TO-116 dual in-line package, with the lead bonds arranged to form the ring demodulator. Comparison of the two quad-FET configurations at operating frequencies through 100 MHz indicated that the single-package arrangement had definitely superior characteristics. Physical assembly into the mixer circuit is easier, and less PC board space is required. Improved performance was noted on the following parameters:

- Lower lead inductance
- Lower distributed capacitance
- Better isolation
- Better rejection of AM noise

All of the mixer performance achievements discussed in this presentation have been made with the single-package quad-FET matrix; it behooves the user to follow this design philosophy, and to limit JFET candidates for selection to those high-performance (high transconductance, low capacitance) devices which are available packaged as matched ring-quad demodulators.

The FET chips used in the single-package configuration were Siliconix U310s, which offer saturated drain current, I_{DSS}, of 20 to 60 mA, and a typical forward transconductance of 18 mmho at $V_{gs} = 0$. Parasitic chip capacitance averages about 4 pF (C_{iss}), which allows for operation well into the UHF region. Table III shows the performance match achieved when adjacent chips were selected from the same wafer.

TABLE III

QUAD-FET CHIP MATCHING

Quad S/N	V_P (V)	I_{DSS} (ma)	g_{fs} (mmho)
04720	3.39	29.2	13.1
	3.54	31.0	12.8
	3.53	30.8	13.0
	3.43	29.4	13.1
04724	3.78	35.6	12.8
	3.74	35.3	12.6
	3.84	35.7	12.7
	3.83	37.2	12.6
04728	5.23	53.4	11.6
	5.14	53.3	11.7
	5.03	51.1	11.5
	5.19	53.3	11.8

All of the quad arrays shown were tested in the mixer assembly, and all provided a maximum dynamic unbalance of only 0.17 dB, ample proof that the practice of adjacent chip selection is valid for close matching.

The pin assignments of the four JFETs in the 14-pin TO-116 dual in-line carrier were arranged to avoid crossovers and maintain sufficient separation between the signal and local oscillator ports to keep stray coupling leakage to a minimum.

Local Oscillator Injection

Local oscillator drive for active FET mixers, either balanced or unbalanced, differs from the drive characteristics of passive diode mixers. In the switching mode, the diode mixer requires sufficient local oscillator drive to swing the diodes from a hard ON state to a hard OFF state. For best IMD performance, the gate of the FET must never be driven positive with respect to the source -- a case equivalent to the hard ON condition of the diode. Consequently, local oscillator drive for the balanced mixer is less than that required for a passive balanced mixer with comparable performance characteristics.

The double-balanced mixer relies on balanced drive from both the local oscillator and the signal source. Since conversion efficiency, optimum noise figure, and good crossmodulation effects can best be served with the signal entering through the common quad JFET source, the local oscillator excitation may be applied directly at the gates of the FET array.

A balanced trifilar-wound toroidal-coil broadband transformer, exhibiting high even-mode rejection, provides the balanced drive for the local oscillator excitation of the quad FET gates. The gates of the quad array have very low conductance; hence there will be some degree of mismatch to the local oscillator, which normally could not be tolerated for the signal port. The high gate impedance, however, allows a moderate level of local oscillator power to bring about the necessary gate voltage swing.

Transformer Design

The design problems encountered in a single-balanced mixer[9] are compounded in the double-balanced mixer: the full-wave JFET quad differs markedly from the half-wave single-balanced JFET pair, in that the quad is represented as a 4-terminal input structure, while the JFET pair is represented as a 2-terminal structure. Consequently, the double-balanced mixer transformer design requires two separate solutions, each offering entirely different structures. While each transformer design will be treated separately, it is important to note the design goals which are common to both.

The transformers must:

(1) Consist of three single-ended terminal pairs, an input and a balanced output;

(2) Offer a broadband match between the unbalanced input and a symmetrical balanced load;

(3) Maintain (over a wide bandwidth) a differential phase of 180° across the symmetrical balanced loads; and

(4) Introduce a minimum of insertion loss.

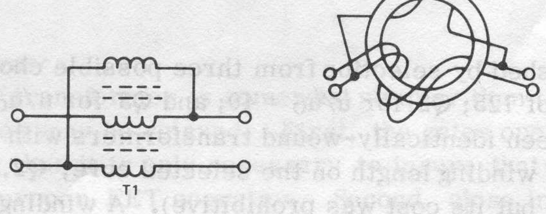
Signal Input Transformer Design

In general, design and fabrication of broadband transformers has been limited to the popular ferrite-core varieties derived from transmission-line theory, [10][11][12] where exceptional bandwidths are possible. The more popular transformer designs frequently result in a 4:1 impedance transformation, as in the single-balanced mixer[13] or in most trifilar designs. Other popular transformers offer either simple constant-impedance phase inversion or unbalanced-to-balanced configurations.

The JFET quad signal input terminals consist of shunt pairs of JFET source terminals which offer a combined load impedance of about 35 Ω as contrasted to a 100 Ω impedance value which would have suited a 4:1 transformer. It was thus necessary to design a broadband unbalanced-to-split-balance transformer which produced, in effect, a 50 Ω asymmetrical input to a 25-0-25 Ω output.

Such a transformer would require an unbalanced 50 Ω input and a symmetrically-balanced output having near-perfect 180° phase differential and an equipotential (even-mode) center tap. Consequently, a two-step design procedure was indicated.

The first step was to design a transformer which would provide the unbalanced-to-balanced transition while maintaining a constant impedance of 50 Ω and a 180° phase differential across the balanced output, over a 50-250 MHz band. The design was straightforward, and is shown schematically in Figure 4. The extra winding was required to complete the necessary magnetization current path.



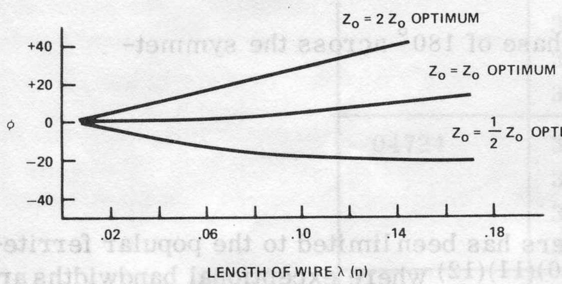
(Figure 4)
Signal Input Transformer

Design of the core windings required selection of the proper ferrite, and establishment of the actual winding length. The latter was resolved to a first-order approximation by the formulas of Pitzalis[14]:

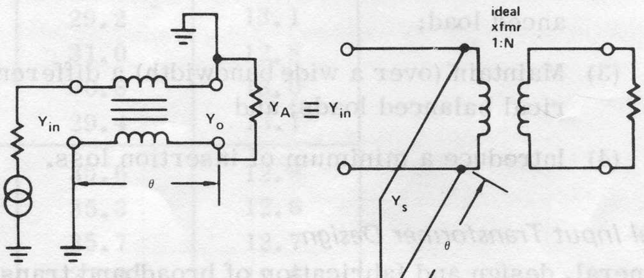
$$\text{max length} = \frac{7200n}{f_{upper}} \quad \text{(inches)} \tag{5}$$

$$\text{min length} = \frac{20\, R_L}{(1 + u/u_o)\, f_{lower}} \quad \text{(inches)} \tag{6}$$

where n = a fractional wavelength determined by the allowable amount of phase error (Figure 5), u/u_o= the relative permeability of the ferrite at the lowest frequency, and R_L = the load impedance.



(Figure 5)
Toroid Coil Winding Data

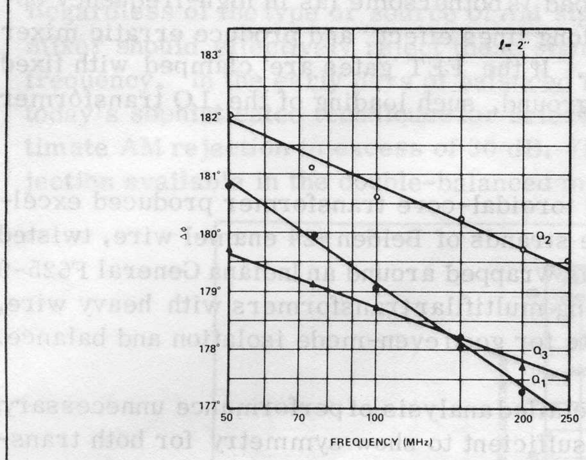


(Figure 6)
Equivalence of Simple Balun

Having established the approximate length limits, the final solution came by experiment. A Hewlett-Packard 8405A vector voltmeter was invaluable during this phase of the work.

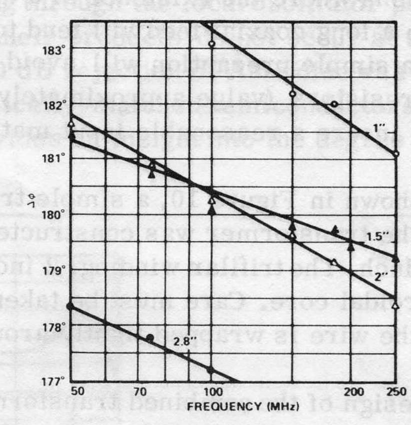
According to Ruthroff[15] the simple balun, to which the signal input transformer can be most readily compared, is equivalent to "an ideal reversing transformer plus a length of transmission line. If the characteristic impedance of the line is equal to the terminating impedance, the transformer is inherently broadband." The true equivalent of the simple Ruthroff balun is shown in Figure 6, where the "length of transmission line" is in effect a shunt element of characteristic admittance, Y_S. If $Y_o = Y_{in} = Y_A$, then it can be shown that $Y_S = Y_A$[16], thus providing a flat admittance transfer through the transformer. Construction of the "ideal reversing transformer" required three turns-per-inch of Belden #24 enamel wire for a characteristic admittance of 0.22 mho[17].

Core permeability was established by selection from three possible choices of Indiana General ferrite (Q1 for a permeability, u/u_o of 125; Q2 for u/u_o = 40; and Q3 for u/u_o = 16). Figure 7A provides a performance comparison between identically-wound transformers with different core permeabilities; Figure 7B shows the effects of winding length on the selected core, Q2. (Core material Q3 might have offered a better permeability, but its cost was prohibitive). A winding length of 1.5 inches was used for this first-stage transformer design. An identical length of single conductor was wound about the core in the same winding direction for the magnetization requirements.



(Figure 7A)

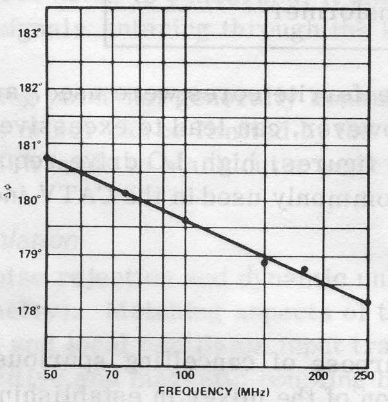
Differences in Core Permeability



(Figure 7B)

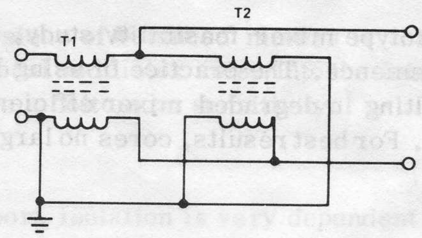
Effect of Winding Length on Core Material

The second phase of the signal input transformer design is to provide a circuit that maintains the precise impedance and phase balance of the reversing transformer, while offering in combination a center-tapped junction with high even-mode rejection. The transformer was wound after the fashion of Ruthroff's 4:1 ratio impedance design [18], with 2 inches of twisted wire on a Q2 core. The resulting transformer, in combination with the reversing transformer discussed earlier, provided the degree of phase balance shown in Figure 8.



(Figure 8)

Input Transformer Phase Balance



(Figure 9)

Completed Signal Input Transformer

The center tap is typically decoupled in excess of 50 dB. The completed signal input transformer is shown in Figure 9. If the design offers the assurance that the center tap will be grounded, then the magnetization winding may be omitted.

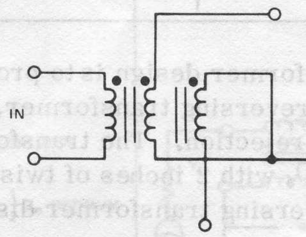
Local Oscillator Input Transformer

Design of the local oscillator transformer is somewhat simpler than that of the signal input transformer, because two design rules may be relaxed. First, the gates operate at a higher impedance than that imposed on the sources; thus it is only necessary to insure that the peak-to-peak voltage swing at the gates is sufficient for proper FET operation. Second, close impedance match is not so critical as in the signal input transformer, since the local oscillator excitation is generally derived directly from a nearby source.

In those situations where the existence of a mismatched load is bothersome (as in high-frequency operation, where a long coaxial feed will tend to exhibit a "long lines effect" and produce erratic mixer performance) a simple precaution will avoid the problem. If the FET gates are clamped with fixed non-inductive resistors (value approximately 200 Ω) to ground, such loading of the LO transformer secondary will insure a reasonable input match.

In the design shown in Figure 10, a simple trifilar-wound toroidal-core transformer produced excellent results. The transformer was constructed from three strands of Belden #24 enamel wire, twisted to 3 turns per inch. The trifilar winding, 2 inches long, was wrapped around an Indiana General F625-9 (CF102) Q2 toroidal core. Care must be taken when winding multifilar transformers with heavy wire, to insure that the wire is wrapped tightly around the ferrite for good even-mode isolation and balance.

Simplicity of design of the combined transformers made detailed analysis of performance unnecessary; indicators such as isolation and dynamic unbalance are sufficient to show symmetry for both transformers and the FET quad.

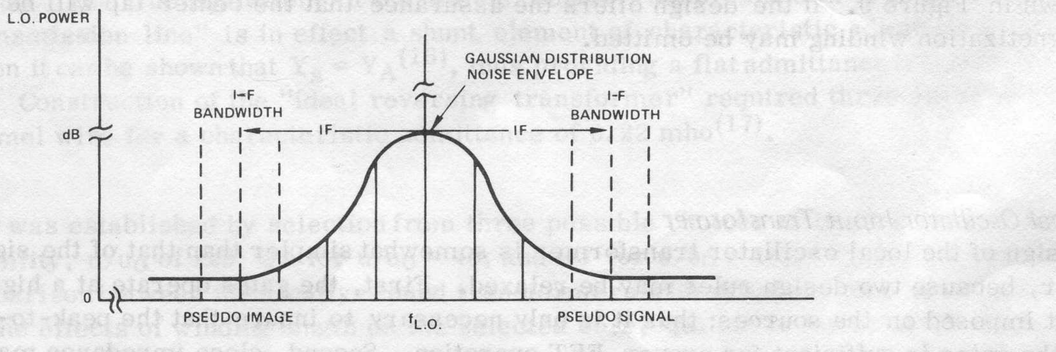


(Figure 10)
Local Oscillator Input Transformer

(For the prototype mixer feasibility study, relatively large ferrite cores were used, as a matter of winding convenience. The practice of using large cores, however, can lead to excessive transformer losses, resulting in degraded mixer efficiency, high noise figures, high LO drive requirements and reduced gain. For best results, cores no larger than those commonly used in the CATV industry should be chosen).

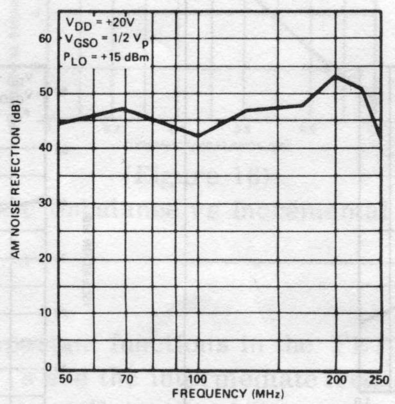
AM Local Oscillator Noise Rejection

Originally, balanced mixers were used for the specific purpose of cancelling spurious AM signals existing on or about the local oscillator carrier (the function of the mixer in establishing good interport isolation was a side-effect).[19] These signals could be either spurious AM signals generated on or about the carrier (Figure 11) or actual signals existing at the signal frequency. In the latter case, the signals enter the mixer through the local oscillator, having found their way in through some leakage coupling phenomenon.



(Figure 11)
Generation of Spurious AM Signals

Regardless of the type or source of AM signals entering through the local oscillator port, the balanced mixer should effectively reject these signals so that their products do not occur at the intermediate frequency. In the early days of balanced mixers, a 20 dB rejection of AM noise was considered good; today's sophisticated techniques for selection of dynamically-matched semiconductors can provide ultimate AM rejection in excess of 30 dB. Figure 12 provides an insight into the degree of AM noise rejection available in the double-balanced mixer.



(Figure 12)
AM Noise Rejection in Double-Balanced Mixer

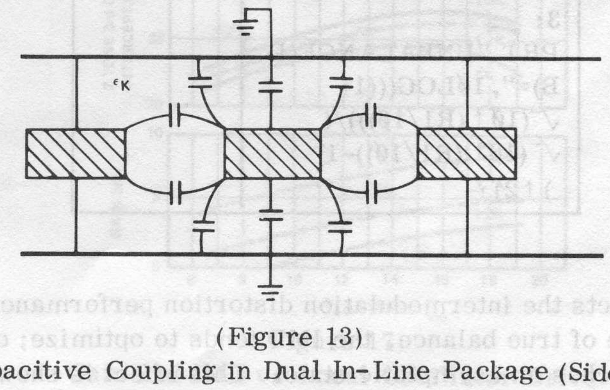
(Insofar as FM noise is concerned, it should be noted that no mixer is capable of rejecting frequency-modulated signals entering through the local oscillator).

An interesting point not generally considered in discussions of balanced mixers is that the dynamic range of the mixer can be limited by the conversion of local oscillator noise into the intermediate frequency, which tends to blank out a weak signal and place a bottom on sensitivity.

Interport Isolation

Like AM noise rejection and dynamic unbalance, interport isolation is very dependent on mixer balance (symmetry). Matching aspects of the JFET quad array and the phase/amplitude balance of the signal input and local oscillator input transformers play important roles in achieving interport isolation. Capacitive and magnetic coupling between the transformers add to problems of interport isolation in balanced mixers.

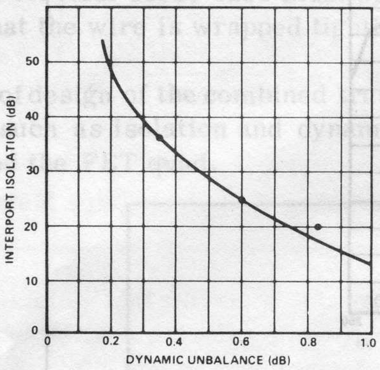
(In the prototype mixer, the JFET quad was packaged in a 14-pin dual in-line housing, as a matter of construction convenience. During tests of the mixer, it was found to be absolutely necessary that alternate pins be grounded to reduce capacitive cross-coupling (Figure 13). It is probable that a more suitable package would have been the 8-pin TO-99, which has insignificant lead capacitance; this packaging approach is recommended for further efforts in construction of the quad FET matrix).



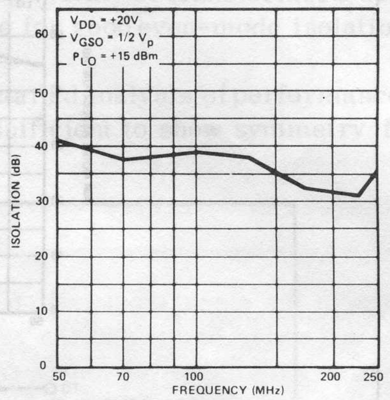
(Figure 13)
Capacitive Coupling in Dual In-Line Package (Side View)

Interport isolation was also enhanced in the prototype mixer through careful parts layout. As a measure of the overall effects of unbalance, a quantitative measurement of interport isolation vs dynamic unbalance is made in Figure 14.

In Figure 15, the interport isolation between the local oscillator and signal input ports is shown to be 35 dB typically.



(Figure 14)
Interport Isolation vs Dynamic Unbalance



(Figure 15)
Interport Isolation

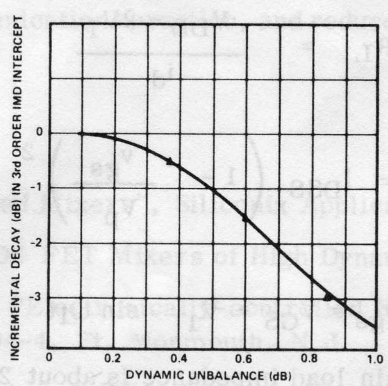
Dynamic Unbalance

Dynamic unbalance may be regarded as another expression for AM noise rejection, except that the latter does not provide a ready insight into the effects of symmetry, balance, and quad match. The algorithm which reduces the measured values of AM noise to dynamic unbalance (via a programmable calculator) is shown in facsimile in Table IV.

TABLE IV

```
0:                          4:
SPC 2; FXD 4 ⊢              SPC 1 ⊢
1:                          5:
ENT "AM REJECT (D           GTO 1 ⊢
B)", R1 ⊢                   6:
2:                          END ⊢
PRT "AM REJ(DB)=
", R1 ⊢
3:
PRT "UNBALANCE(D
B)=", 1ØLOG(((1+
√(1Ø ↑ (R1/1Ø)))/(
√ (1Ø↑ (R1/1Ø))-1)
) ↑ 2) ⊢
```

Dynamic unbalance also effects the intermodulation distortion performance of the mixer. As the unbalance approaches a degree of true balance, the IMD tends to optimize; conversely, when unbalance is excessive the IMD approaches an asymptotic state. This effect is shown in Figure 16.



(Figure 16)
Dynamic Unbalance vs Incremental Decay

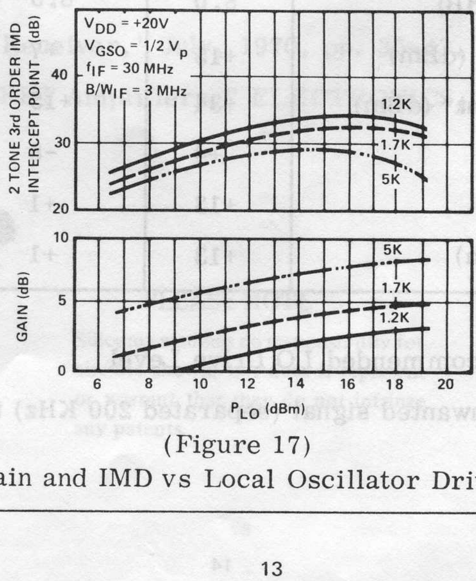
Designing the IF Network

The IF network performs three important functions in the FET double-balanced mixer. It provides for best match between the quad FETs and the intermediate frequency amplifier; it effectively bypasses the RF components (signal and local oscillator); and it provides a reduction of simple harmonic distortion, by virtue of its balance.

In any mixer design, all RF components must be bypassed for best conversion efficiency (any energy not "converted" by mixing action will reduce conversion gain). RF bypassing also prevents spurious resonances and other undesired phenomena from affecting mixer performance. Generally, 20 dB of isolation is adequate, although most passive double-balanced mixers -- as well as the prototype active FET mixer -- can offer greater than 40 dB.

The IF network uses the well-known pi match structure to provide a narrow-band IF output, serving three functions. It achieves the proper drain load impedance match between the FETs and the IF structure. It provides the necessary isolation between the RF components and the intermediate frequency. And it serves as a simple three-pole filter which provides a monotonic decrease in the drain impedance as the frequency departs from the center frequency, f_{if}, which also adds to the suppression of harmonic distortion products.[20]

Selection of the dynamic drain impedance value in the IF network is a critical point in the design of the structure. Both IM product distortion and cross-modulation will be affected by the instantaneous peak-to-peak voltage of the FETs if the dynamic drain impedance allows the signal peaks to enter either the pinchoff or breakdown voltage regions of the transistors[21]. Here another design tradeoff must be considered. If the impedance is too high, the dynamic range of the mixer will be limited; if the impedance is too low, useful conversion gain will be sacrificed, as shown in Figure 17.



(Figure 17)
Gain and IMD vs Local Oscillator Drive

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2V_P}{i_d} \tag{7}$$

where

$$i_d = I_{DSS}\left(1 - \frac{v_{gs}}{V_p}\right)^2 \tag{8}$$

and

$$v_{gs} = V_{GS} + V_1 \sin \omega_1 t \tag{9}$$

For the FET quad, the optimum drain load impedance is about 2,000 Ω, with the gate bias at one-half pinchoff, and the local oscillator drive at a nominal +15 dBm.

The coupling structure is an 800 Ω CT to 50 Ω transformer (Relcom BT-9). Through various pi-transformations and comparative IMD and gain measurements, an operating Q of 10 was established to insure that the tolerance of the components would permit the IF output to peak within the allowable bandwidth of the IF amplifier.

Mixer Performance

Quad FET arrays with both high and low pinchoff voltage levels were used in evaluation of the active double-balanced mixer; the prototype mixer exhibited clearly superior characteristics, compared to equivalent small-signal passive double-balanced mixers. The low- to medium-level pinchoff voltage quad FET array performed slightly better than the high-level pinchoff devices (5.5 V), solely because of a limitation in available local oscillator power. Performance of several types of mixers is made in Table V.

TABLE V

Comparison Between Active, Passive, and MOS-FET Double-Balanced Mixers

Characteristic	Active FET	Passive Low-Level	Passive High-Level	MOS-FET Switch
Frequency Range (MHz)	50-250	0.5-500	0.5-500	0.2-100
AM Local Oscillator Noise Rejection(dB)	45	Unknown	Unknown	Unknown
Dynamic Unbalance (dB)	0.15	Unknown	Unknown	Unknown
Isolation RF-Local Oscillator (dB)	35	35	40	30
Isolation Local Oscillator - RF (dB)	60	25	30	25
Overall Noise Figure (SSB) (dB)	8.0	8.5	8.5	9.0
Local Oscillator Drive Level (dBm)	+15	+7	+17	+30
Two-Tone IMD Intercept Point* (dBm)	+34	+15	+28	+30
Conversion Gain (dB)	+4	-8	-8	-9
1 dB Compression (dBm)	+13	+1	+8	+27***
Desensitization Level** (dBm)	+13	+1	+8	Unknown

* Output - Measured at Recommended LO Drive Level

** The level for a nearby unwanted signal (separated 200 KHz) to compress a desired signal of -15 dBm by 1 dB

*** Estimated

Conclusion

It may be concluded that performance of the active double-balanced mixer contributes overall system gain in areas critical to telecommunications practice, and reduces associated amplifier requirements.

References

(1) Oxner, E., "FETs in Balanced Mixers", Siliconix Application Note, July, 1972.

(2) Rafuse, R., "Symmetric MOS FET Mixers of High Dynamic Range," ISSCC, 1968.

(3) Brader, Dawson and Sheldon, "Electronically-controlled High Dynamic Range Tuner," Final Report, June, 1971, ECOM-0104-4, Ft. Monmouth, N.J.

(4) "MOS Devices for Linear Systems" RCA Engineer, Oct/Nov., 1971.

(5) J. C. Hoigaard, "Spurious Frequency Generation in Frequency Converters," MICROWAVE JOURNAL, Vol. 11, July/August, 1967.

(6) D. H. Westwood, "Rid Mixers of Spurious Signals,", ELECTRONIC DESIGN, Aug. 16, 1966, p. 210 ff.

(7) Op. cit., "FETs in Balanced Mixers," p. 6.

(8) Op. cit., "FETs in Balanced Mixers," p. 7.

(9) Op. cit., "FETs in Balanced Mixers," pp. 8-10.

(10) C. L. Ruthroff, "Some Broadband Transformers", Proc IRE, Vol. 47, Aug. 1959, pp. 1137-1342.

(11) R. E. Matick, "Transmission Line Pulse Transformers," Proc IEEE, Vol. 56, January 1968, pp. 47-62.

(12) O. Pitzalis and T. Couse, "Broadband Transformer Design for RF Power Transistor Amplifiers," Proceedings Electronic Components Conference, 1968.

(13) Op. cit., "FETs in Balanced Mixers," pp. 8-10.

(14) Op. cit., "Broadband Transformer Design for RF Power Transistor Amplifiers,"

(15) Op. cit., "Some Broadband Transformers."

(16) Matthaei, G. L., Young, L., and Jones, E. M. T., Microwave Filters, Impedance Matching Networks, and Coupling Structures, Ch. 5, McGraw-Hill, New York, N.Y., 1964.

(17) P. Lefferson, "Twisted Magnet Wire Transmission Line," IEEE Transactions (Parts, Hybrids, and Packaging), Vol. PHP-7, No. 4, December, 1971.

(18) Op. cit., "Some Broadband Transformers," Figure 6(a).

(19) Pound, R. V., MICROWAVE MIXERS, MIT Rad. Lab. Series, Vol. 16, p. 257, McGraw-Hill, Inc., New York, N.Y. 1948.

(20) Sabin, W., "The Solid State Receiver," July, 1970, pp. 35-43.

(21) Sherwin, J., "Distortion in FET Amplifiers," ELECTRONICS, December 12, 1966.

[redacted]

PLEASE NOTE

Siliconix assumes no responsibility for circuits shown, nor does it represent or warrant that they do not infringe any patents.