DESIGNING FET BALANCED MIXERS FOR HIGH DYNAMIC RANGE

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Central Applications

SECTION 1: FETS IN SINGLE BALANCED MIXERS

INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

Table 1

Characteristic	MIXER TYPE		
	Single-Ended	Single Balanced	Double Balanced
Bandwidth	Several decades possible	Decade	Decade
Relative 1M Density	1.0	0.5	0.25
Interport Isolation	Little	10-20 dB	>30 dB
Relative L. O. Power	0 dB	+3 dB	+6 dB

Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

Table 2

DEVICE	ADVANTAGES	DISADVANTAGES
Bipolar Transistor	Low Noise Figure High Gain Low D.C. Power	High IM Easy Overload Subject to Burnout
Diode	Low Noise Figure High Power Handling High Burn-out Level	High L. O. Drive Interface to I.F. Conversion Loss
JFET	Low Noise Figure Conversion Gain Excellent IM products Square Law Characteristic Excellent Overload High Burn-out Level	Optimum Conversion Gain Not Possible at Optimum Square Law Response High Lo Power
Dual-Gate MOS FET	Low IM Distortion AGC Squre Law Characteristic	High Noise Figure Poor Burnout Level

Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).

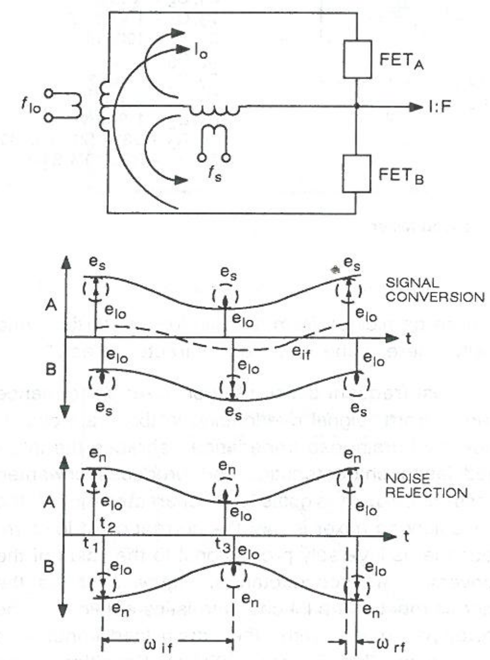

Figure 1. Signal and Noise Vectors

Energy conversion into the intermediate frequency (IF) pass-band is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate (ω_{ift}); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time (t_1) the noise component (e_n) is "in phase" with the local oscillator vector (e_{lo}) and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time t_2, the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced 180° (ω_{ift}) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise[1].

The analysis of the conversion of the signal to the IF pass-band is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time t_2, the signal vector (e_s) is "out of phase" with the local oscillator vector, e_{lo}. The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a prototype balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

1. Intermodulation and Cross-Modulation
2. Conversion Gain
3. Noise Figure
4. Selecting the Proper FET
5. Local Oscillator Injection
6. Designing the Input Transformer
7. Designing the IF Network

Intermodulation and Cross-Modulation

A basic aim in mixer design is to avoid the effects of intermodulation product distortion and cross-modulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both cross-modulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest[2].

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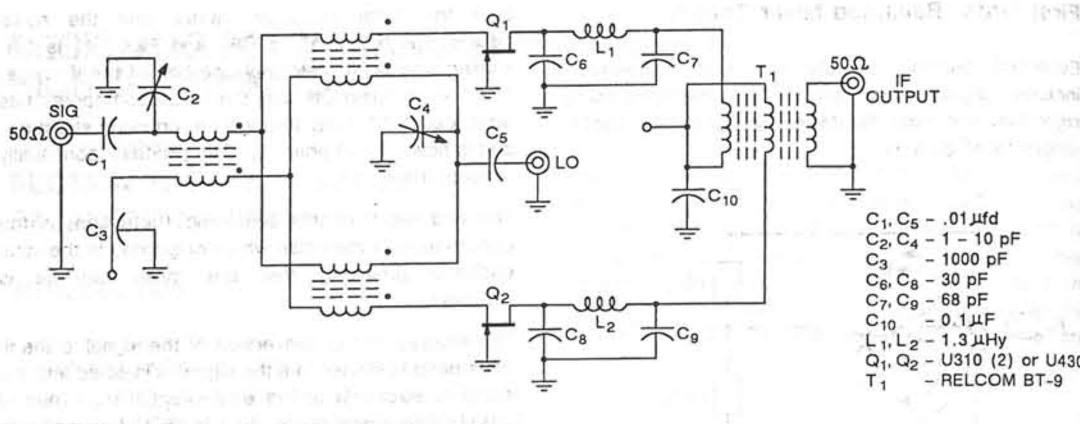

Figure 2. Prototype Active Balanced Mixer

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an n-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance, g_c, is achieved at about 80% of the FET gate cutoff voltage, $V_{GS(off)}$, and amounts to about 25% of the forward transconductance, g_{fs}, of the FET when used as an amplifier. Since conversion gain (or loss) must be considered, it is common to equate voltage gain A_V, as:

$$A_V = g_c R_L \tag{1}$$

where g_c is the conversion transconductance and R_L is the FET drain load.

An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion - particularly intermodulation product distortion.

Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called "varactor effect."

The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted cross-modulation signals[3]. A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in the IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated ("triode") region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 21 through 23.

Distortion from the "varactor effect" is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-source voltage can cause a change in parasitic capacitance, C_{rss}, and give rise to harmonics[4]. A FET tends to be voltage-dependent when the drain voltage falls appreciable below 6 volts. If the source voltage (from the power supply) is also low and the drain load impedance in high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.

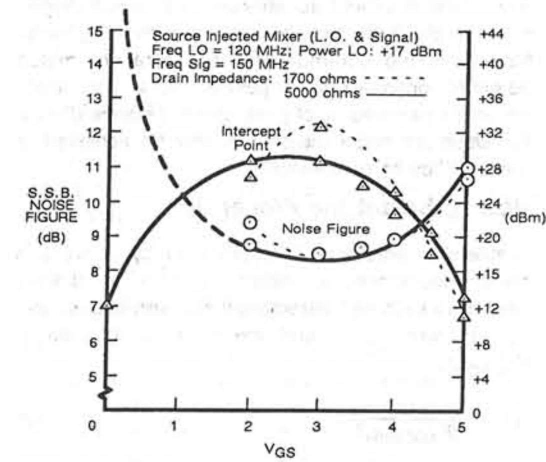

Figure 3. Comparison of Mixer IM Characteristics

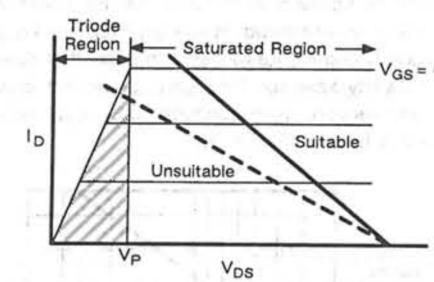

Figure 4. Plotting Drain Load Lines

Conversion Gain

In a FET, forward transconductance is defined as

$$g_{fs} = \frac{dI_D}{dV_{gs}} \tag{2}$$

and conversion transconductance is defined as

$$g_c = \frac{dI_D(\omega i)}{dV_{gs}(\omega r)} \tag{3}$$

where ωi = the intermediate frequency and ωr = the signal frequency.

The effects of time-varying local oscillator voltage, V_2, and the much smaller signal voltage, V_1, must be considered:

$$V_{gs} = V_1 \cos\omega_1 t + V_2 \cos\omega_2 t \tag{4}$$

For square law operation

$$V_2 + V_{GS} \leq V_{GS(off)} \tag{5}$$

Drain current is approximately defined by

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \tag{6}$$

or

$$I_D \approx \frac{g_{fso} V_{GS(off)}}{2}\left[1 - \frac{V_{gs}}{V_{GS(off)}}\right]^2 \tag{7}$$

or

$$I_D \approx \frac{g_{fso}}{2\,V_{GS(off)}}\left[V_{GS(off)} - V_{gs}\right]^2 \tag{8}$$

then

$$I_D \approx \frac{g_{fso}}{2\,V_{GS(off)}} \text{ (complex Taylor expansion)} \tag{9}$$

which can be reduced

$$I_{D(IF)} \approx \frac{g_{fso}}{2\,V_{GS(off)}} V_1 V_2 \cos(\omega 1 - \omega 2)\,t \tag{10}$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2\,V_{GS(off)}} |V_2| \tag{11}$$

Equation 11 suggests that g_c increases without limit as V_2 increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of V_2 should not exceed $V_{GS(off)}$.

Thus

$$2\,V_2 \text{ peak} \leq V_{GS(off)} \tag{12}$$

or

$$V_2 \text{ peak} \leq \frac{V_{GS(off)}}{2} \tag{13}$$

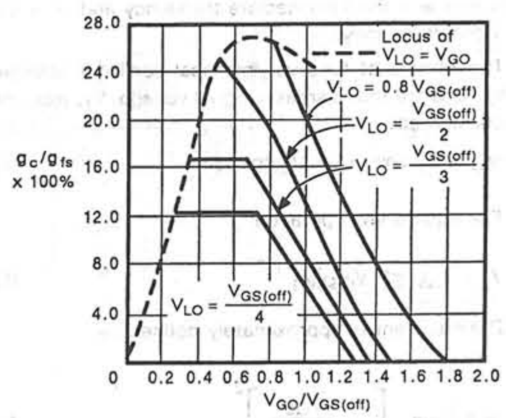

Figure 5. Normalized g_c/g_f vs. $V_{GS}/V_{GS(off)}$ (from "FET RF Mixer Design Technique", S.P. Kwok, WESCON Convention Record (1970) 8/1, p.2.) Used with Permission

Figure 5 shows plots of normalized conversion transconductance, g_c/g_{fs} versus normalized quiescent bias, $V_{GS}/V_{GS(off)}$, for different oscillator injections.

Noise Figure

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance, R_g [5]. A change of a decade in R_g can produce a noise figure variation of as much as 3 dB.

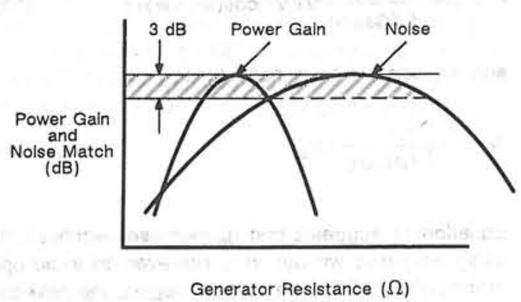

Figure 6. Power Gain and Noise Matching

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance, g_{igs}, which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.

How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance, g_c, which in turn is directly related to such FET parameters are zero-bias saturation current, I_{DSS}, and the gate cutoff voltage, $V_{GS(off)}$:

$$g_c = \frac{I_{DSS}}{2\,V_{GS(off)}^2}\,|V_2| \tag{14}$$

$$\approx \frac{g_{fso}}{2\,V_{GS(off)}}\,|V_2| \tag{15}$$

Equation 14 appears to indicate that FETs with high I_{DSS} are to be preferred. However, I_{DSS} and $V_{GS(off)}$ are related, and Figures 7a and 7b show that devices from a family selected for high I_{DSS} do not provide high conversion transconductance, but actually produce a lower value of g_c.

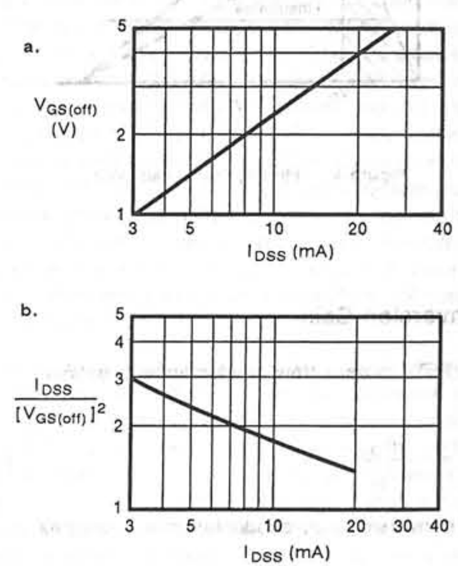

Figure 7. Relationship of I_{DSS} and $V_{GS(off)}$

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS}, for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 14,000 mmhos typical at $V_{DS} = 10$ V, $I_D = 10$ mA, and f = 1 kHz.

Criteria for FET Selection

In balanced mixers using FETs, conversion efficiency of the devices is determined by conversion transconductance, g_c, which in turn is directly related to such FET operating parameters as zero-bias drain current, I_{DSS}, and gate cutoff voltage, $V_{GS(off)}$.

It can be shown that

$$\frac{I_{DSS}}{2\,V_{GS(off)}^2}\,\left|V_2\right| \approx \frac{g_{fso}}{2\,V_{GS(off)}}\,\left|V_2\right| \tag{16}$$

where V_2 is the time-varying local oscillator voltage. To maintain operation in the square-law region, we repeat Equation 13,

$$V_2\ \text{(peak)} \leq \frac{V_{GS(off)}}{2} \tag{17}$$

where now, under optimum performance conditions, we merge Equation 11 with Equation 13 to find

$$g_c \approx \frac{g_{fso}}{2\,V_{GS(off)}}\,\frac{V_{GS(off)}}{2} = \frac{g_{fso}}{4} \tag{18}$$

which agrees with Equation 15.

For the highest level of conversion transconductance, it would appear initially that for any given FET geometry, units with high I_{DSS} are to be preferred. But as we saw in Figure 7, since I_{DSS} and $V_{GS(off)}$ are related, a performance tradeoff is necessary; however, an increased value of I_{DSS} provides increased dynamic range. Since balanced mixer design involves many tradeoffs for best performance, this I_{DSS} vs. $V_{GS(off)}$ problem is generally inconsequential.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach - the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310 (Table 3). Remember, however, that conversion transconductance, g_c, can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure.

Table 3

Typical Characteristics	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	15 K	6 K	5 K	3.5 K
I_{DSS}	40 mA	15 mA	10 m	10 mA

*Similiar products are available in TO-92:
U310 (J310)
2N4416 (2N5486)

Local Oscillator Injection

Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5. V_{LO} is expressed in terms of peak-to-peak voltage, while $V_{GS(off)}$ is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing. Two circuits to obtain direct gate coupling are suggested in Figure 8.

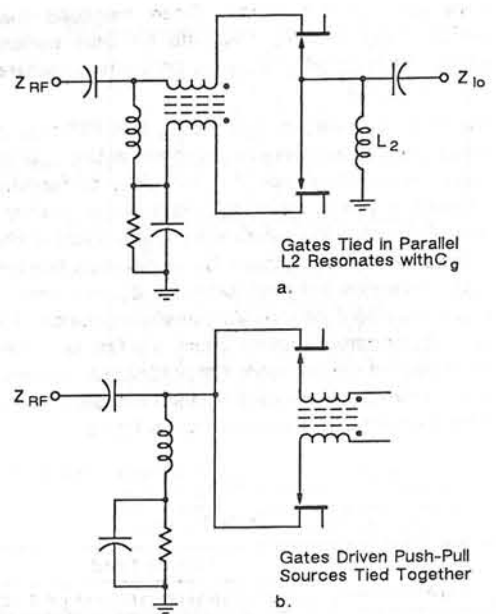

Figure 8. Alternate Forms of L.O. Injection

The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer, best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-Ω load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

Designing the Input Transformer

Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

1. Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B
2. Offer a match between either input to a symmetrical balanced load
3. Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)
4. Maintain a differential phase of 180° across the symmetrical balanced loads
5. Introduce the least possible amount of loss

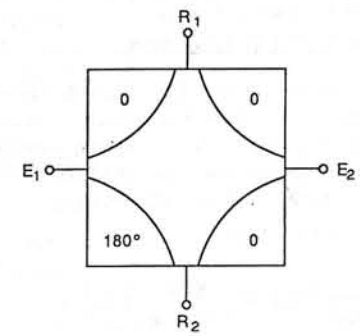

Figure 9. 4-Port Hybrid with Phase and Isolation

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite. The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff [6].

Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis[7]. The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{upper}} \text{ (inches)} \qquad (19)$$

$$\text{min length} = \frac{20R_L}{(1+\mu/\mu_o)\, f_{lower}} \text{ (inches)} \qquad (20)$$

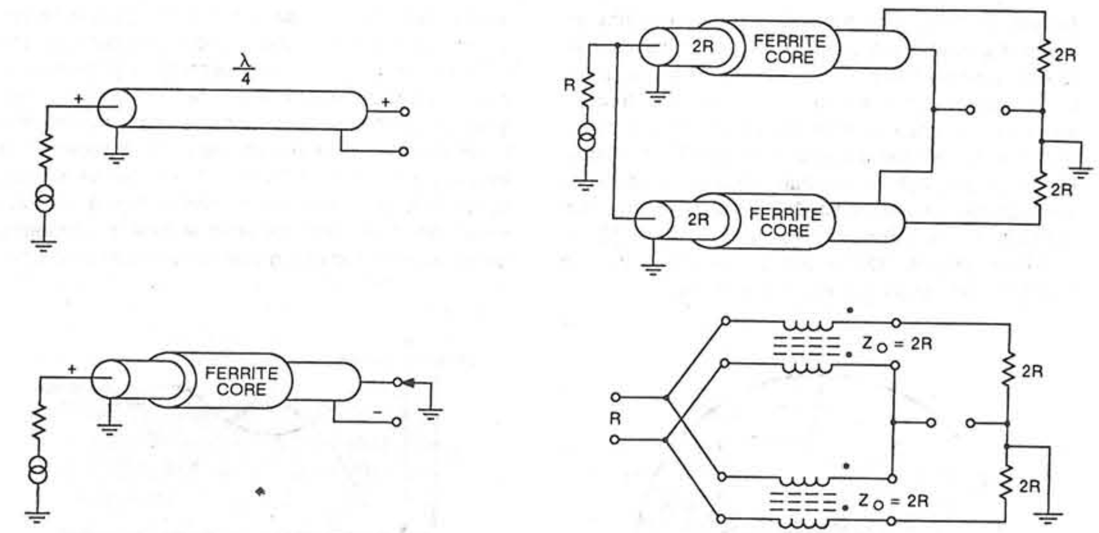

Figure 10. Hybrid Input Coupling Transformer

where R_L = the load impedance, $\mu/\mu o$ = the relative permeability of the ferrite at the lower frequency, and n = a fractional wavelength determined by the amount of allowable phase error.

Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high Q.

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium. A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line conductors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance, Z_O, is to be preferred over a higher Z_O. Both 50-Ω and 100-Ω transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45 Ω is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while 3½ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide Z_O = 100 Ω. Each core is wound with 2 inches of proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 19,20).

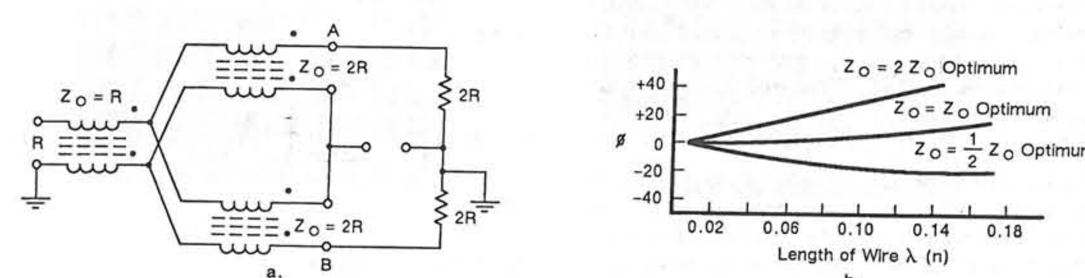

Figure 11. Toroid Coil Winding Data

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As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated (C_2, C_4, Figure 2). A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within ±2 degrees (about 180°) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) – but phase track beyond 250 MHz *may* show too much deterioration.

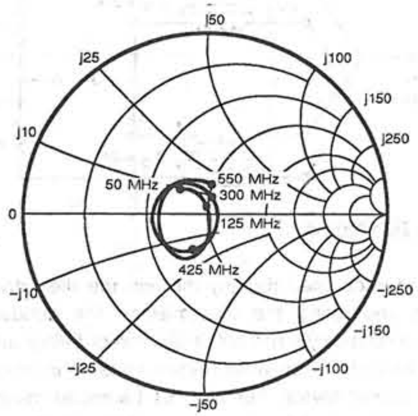


Figure 12. 50 Ω - 200 Ω Balun

Designing the IF Network for Single-Balanced Mixers

The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi (π) match structure from each FET drain to a common balanced output transformer network. This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency, f_o[8]. This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

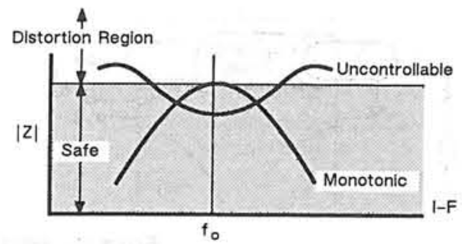


Figure 13. Pi (π) Match Filter Function

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and cross-modulation will be both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors. If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2\,V_{GS(off)}}{i_d} \qquad (21)$$

where

$$i_d = I_{DSS}\left[1 - \frac{V_{gs}}{V_{GS(off)}}\right]^2 \qquad (22)$$

and

$$V_{gs} = V_{GS} + V_1 \sin \omega_1 t \qquad (23)$$

For the U310 FET, the optimum drainload impedance is established at slightly less than 2000 Ω, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-Ω CT to 50-Ω trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 Ω on each FET; excellent IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

Single-Balanced Mixer Performance

Tests of the operational prototype FET single-balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table 4 (measurements of all three mixers were made under laboratory conditions).

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point[9]. With two signals 300 kHz apart, the balanced mixer suppressed third-order products -89 dB with both signals at -10 dB, representing an intercept point of +32 dBm.

Table 4

50-150 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dB	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8.5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+2.5 dB*	-6 dB	+18 dB
Single-sideband Noise Figure @ 50 MHz	7.2 dB	6.5 dB	6.0 dB

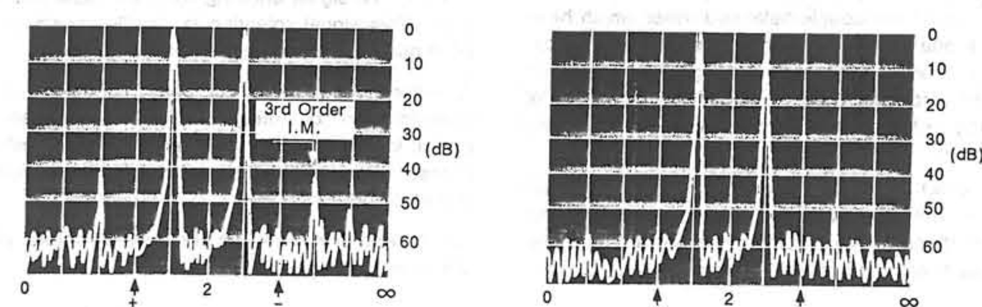
* Conservative minimum † Estimated

Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.

CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed



Schottky-Barrier Double Balanced Mixer

JFET Balanced Mixer

Figure 14. Comparison of 3rd Order IM Products

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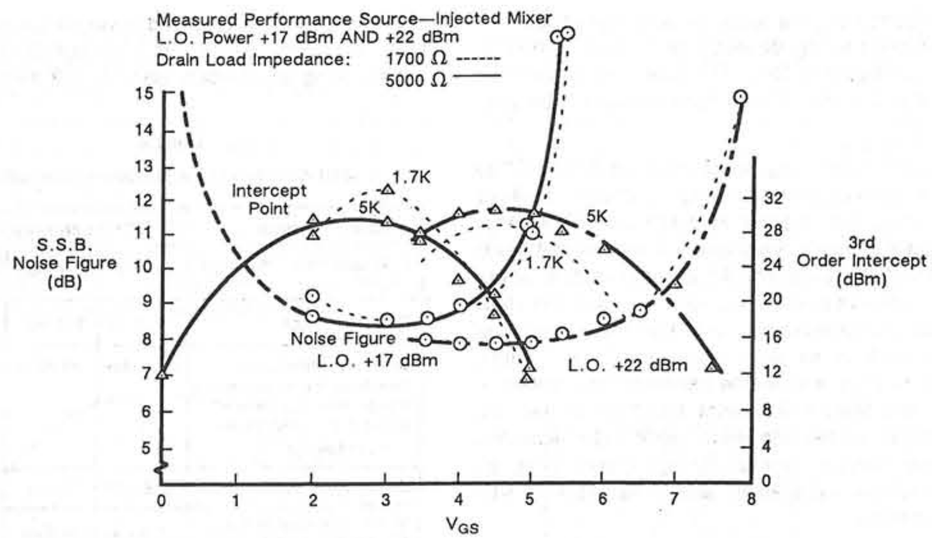

Figure 15. Noise Figure and Intercept Point Performance Single-Balanced Mixer

from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 19 and 20) are equally applicable to trifilar as they are for bifilar.

SECTION 2: JUNCTION FETS IN DOUBLE-BALANCED MIXERS

INTRODUCTION

Dynamic range is probably the most important consideration in modern receiver design. Table 1 provides a comparison between the harmonic distortion characteristics of a simple mixer, a single-balanced mixer, and a double-balanced mixer. The comparison clearly shows those performance characteristics of the double-balanced mixer which have made it one of the most popular of all mixer types. Among these attributes are greatly improved interport isolation and a significant degree of rejection of local oscillator carrier amplitude modulation.

When used in double-balanced mixers, however, passive devices such as Schottky-barrier (hot carrier) diodes have certain fundamental shortcomings, such as high conversion loss and high local oscillator drive requirements. Thus the active balanced mixer which employs field-effect transistors is a welcome innovation: conversion gain and improved intermodulation distortion characteristics alone place the FET double-balanced mixer far ahead of its passive counterparts. The high saturation levels possible with modest local oscillator power make such a mixer useful for mixing both small and large signals.

First Order Double-Balanced Mixer Theory

In either single or double-balanced mixer design, the prime requirement is that when the mixer is excited by the local oscillator carrier, the circuit must be capable of rejecting the amplitude-modulated wave which exists about the L.O. Also, the mixer must reject any AM signal entering from the local oscillator port. (This signal rejection is usually known as AM local oscillator noise cancellation).

A second requirement for balanced mixers is the establishment of interport isolation between the signal, local oscillator, and IF ports. A third desirable characteristic is the reduction of intermodulation distortion products.

Careful attention to design of double-balanced mixers will satisfy the foregoing criteria.

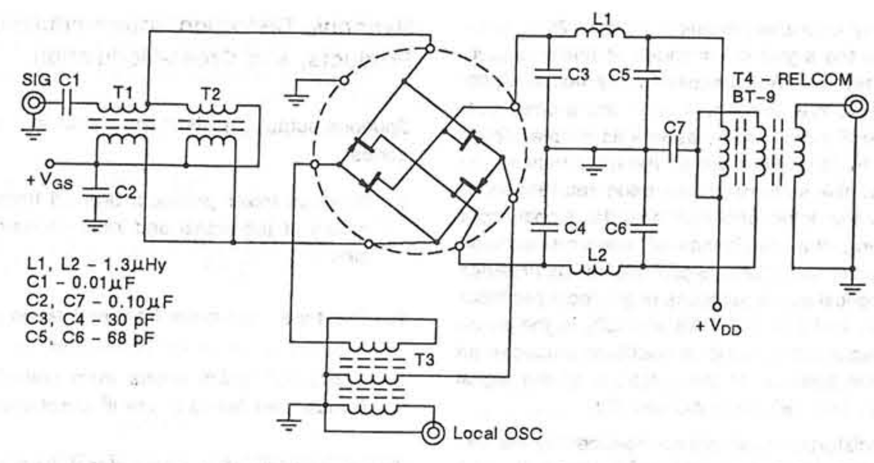

Figure 16. Double-Balanced Mixer

The schematic of a prototype double-balanced mixer (Figure 16) employs four high-performance junction FETs chosen for closely matched characteristics. (The significance of the quad-FET configuration will be dealt with later).

If the schematic in Figure 16 is reduced to show only the local oscillator circuit (Figure 17a), the rejection mechanism of AM signals, either on the L.O. carrier on entering through the local oscillator port, is readily understood.

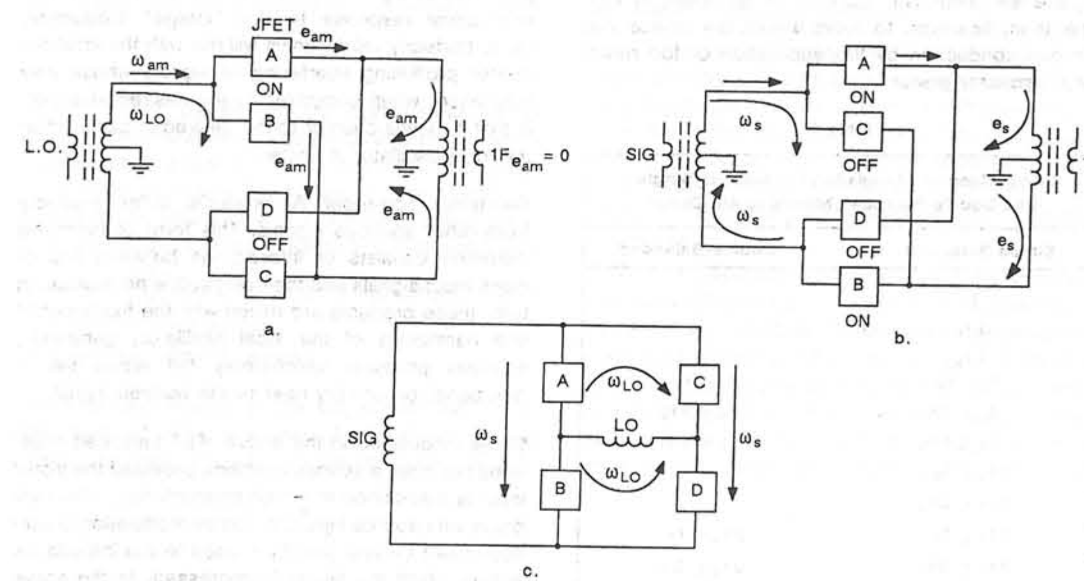

Figure 17.

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Likewise, the equivalent circuit in Figure 17b demonstrates how the signal is enhanced at the IF output. Both local oscillator AM cancellation, as well as signal enhancement, are dependent upon the precise balance of the IF transformer, as well as on the match of the four FETs which make up the quad network. In Figure 17c, the schematic has been rearranged to show both the local oscillator and the signal input transformers; the mechanics of interport isolation may be easily visualized. Signal excitation provides an equipotential at the junctions of the local oscillator transformer and FET pairs AB and CD; in the same manner, excitation of the local oscillator produced an equipotential balance at the junctions of the signal transformer and FET pairs AC and BD.

Harmonic distortion products are reduced by the balance between the signal and local oscillator (inputs) and the IF (output), where even-integer harmonics of the signal and local oscillator frequencies are effectively canceled. A sixth-order summary of such products in both single- and double-balanced mixers is shown in Table 5. Note how the relative densities agree with Table 1. The effects of harmonic distortion can be reduced by a judicious selection of the IF passband response[10]. Third-order IMD (Intermodulation Distortion) products are reduced by virtue of the characteristics of junction FETs, which approximate a square-law response. Care must be taken in FET operation, however, to avoid driving the device into forward conduction by the application of too much local oscillator power.

Table 5

Comparison of Modulation Products in Single and Dougle Balanced Mixers to 6th Order

Single-Balanced	Double-Balanced
f_s	
$3 f_s$	
$5 f_s$	
$f_o \pm f_s$	$f_o \pm f_s$
$f_o \pm 3 f_s$	$f_o \pm 3 f_s$
$f_o \pm 5 f_s$	$f_o \pm 5 f_s$
$2 f_o \pm f_s$	
$2 f_o \pm 3 f_s$	
$3 f_o \pm f_s$	$3 f_o \pm f_s$
$3 f_o \pm 3 f_s$	$3 f_o \pm 3 f_s$
$4 f_o \pm f_s$	
$5 f_o \pm f_s$	$5 f_o \pm f_s$

Harmonic Distortion, Intermodulation Products, and Cross-Modulation

Spurious output signals in mixers fall into three categories:

1. Spurious mixer products derived from harmonic mixing of the signal and local oscillator frequencies;
2. Two-tone, odd-order intermodulation products;
3. "Chirping" which arises from undesired mixing frequencies falling in the IF passband.

The harmonics of a single-signal frequency, when mixed with the harmonics of the local oscillator, produce spurious outputs which are level-dependent on the signal amplitude. These products are greatly reduced by the double-balanced mixer, where the even harmonics are effectively canceled; when FETs are used, the Taylor-series power expansion falls quickly to zero above the second order.

However, modulation products of a similar nature will arise if the broadband down-converting mixer is not preceded by signal preselection, because of the mixer's equal response to the "image" frequency. Here, perfectly valid signals will mix with the local oscillator producing interfering i-f signals whose only difference, when compared to the desired i-f signal, is that it moves counter to the desired i-f signal when the local oscillator is shifted.

Two-tone, odd-order IM products differ markedly from other spurious signals. This form of harmonic distortion consists of interactions between two or more input signals and their respective harmonics. In turn, these products are mixed with the fundamental and harmonics of the local oscillator, generating spurious products which may fall within the IF passband, on or very near to the desired signal.

Cross-modulation in the active JFET balanced mixer does not pose a serious problem, provided the signal input is maintained at a high conductance, which will occur with source injection. Cross-modulation is very dependent on and directly related to the impedance across which the signal is impressed. In the active JFET double-balanced mixer this impedance is very low, typical 35 Ω. Consequently, the effects of cross-modulation may be disregarded.

In the mixing process of any active device, the value of the FET drain current may be derived from a knowledge of the transconductance of the device, and the impressed signal voltage, e_g. This is obtained from the Taylor-series power expansion:

$$I_d = g_m e_g + \frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2 + \frac{1}{3!}\frac{\delta^2 g_m}{\delta V_G^2} e_g^3 \ldots \frac{1}{n!}\frac{\delta^{n-1} g_m}{\delta V_G^{n-1}} e_g^n \qquad (24)$$

which can be reduced to the terms in Table 6.

Table 6

Term	Output	Transfer Characteristic
$g_m e_g$	F1, F2	Linear
$\frac{1}{2!}\frac{\delta g_m}{\delta V_G} e_g^2$	2 F1, 2 F2 F1 ± F2	Second-order Square-law
$\frac{1}{3!}\frac{\delta g_m}{\delta V_G^2} e_g^3$	3 F1, 3 F2 2 F1 ± F2 2 F2 ± F1	Third order

In FET theory, the second and higher-order derivatives of g_m are absent, and the device thus offers a considerable reduction of both intermodulation products and higher-order harmonics. In the double-balanced mixer, where F1 = F2 is the desired result, it is well to manipulate mixer design and bias conditions to render $\frac{\delta g_m}{\delta V_G}$ as large as possible, simultaneously reducing all other terms.

Criteria for FET Selection

For best performance in the single-balanced mixer, matched FET pairs were used. A 10% match in gate cutoff voltage, $V_{GS(off)}$, saturated drain current, I_{DSS}, and forward transconductance was sufficient; a wide selection of junction FET pairs is available for single-balanced mixer applications. However, in a double-balanced mixer using a ring-style (quad) demodulator, the match must be extended to four discrete devices. Although high forward transconductance remains desirable, the selection of FETs becomes sharply limited for most users.

Early in the development of the prototype double-balanced mixer, evaluation was made of the potential effect of physical FET packaging on mixer performance. Four selected discrete JFETs were arranged in a matrix which was electrically and schematically identical to the circuit shown in Figure 16. At the same time, four FET chips were mounted in a TO-116 dual in-line package, with the lead bonds arranged to form the ring demodulator. Comparison of the two quad-FET configurations at operating frequencies through 100 MHz indicated that the single-package arrangement had definitely superior characteristics. Physical assembly into the mixer circuit is easier, and less PC board space is required. Improved performance was noted on the following parameters:

- Lower lead inductance
- Lower distributed capacitance
- Better isolation
- Better rejection of AM noise

All of the mixer performance achievements discussed in this presentation have been made with the single-package quad-FET matrix; it behooves the user to follow this design philosophy, and to limit JFET candidates for selection to those high-performance (high transconductance, low capacitance) devices which are available packaged as matched ring-quad demodulators.

The FET chips used in the single-package configuration were Siliconix U310s, which offer saturated drain current, I_{DSS}, of 20 to 60 mA, and a typical forward transconductance of 14 mmho at $V_{GS} = 0$. Parasitic chip capacitance averages about 4 pF (C_{iss}), which allows for operation well into the UHF region. Table 7 shows the performance match achieved when adjacent chips were selected from the same wafer.

Table 7

Quad-FET Chip Matching			
Quad S/N	$V_{GS(off)}$ (V)	I_{DSS} (ma)	g_{fs} (m℧)
04720	3.39	29.2	13.1
	3.54	31.0	12.8
	3.53	30.8	13.0
	3.43	29.4	13.1
04724	3.78	35.6	12.8
	3.74	35.3	12.6
	3.84	35.7	12.7
	3.83	37.2	12.6
04728	5.23	53.4	11.6
	5.14	53.3	11.7
	5.03	51.1	11.5
	5.19	53.3	11.8

All of the quad arrays shown were tested in the mixer assembly, and all provided a maximum dynamic unbalance of only 0.17 dB, ample proof that the practice of adjacent chip selection is valid for close matching.

The pin assignments of four JFETs in the 14-pin TO-116 dual in-line carrier were arranged to avoid crossovers and maintain sufficient separation between the signal and local oscillator ports to keep stray coupling leakage to a minimum. Siliconix offers the U350, a quad-ring demodulator consisting of matched U310 JFETs.

Local Oscillator Injection

Local oscillator drive for active FET mixers, either balanced or unbalanced, differs from the drive characteristics of passive diode mixers. For best IMD performance, the gate of the FET must never be driven positive with respect to the source - - a case equivalent to the hard ON condition of the diode. Consequently, local oscillator drive for the balanced mixer is less than that required for a passive balanced mixer with comparable performance characteristics.

The double-balanced mixer relies on balanced drive from both the local oscillator and the signal source. Since conversion efficiency, optimum noise figure, and good cross-modulation effects can best be served with the signal entering through the common quad JFET source, the local oscillator excitation may be applied directly at the gates of the FET array.

A balanced trifilar-wound toroidal-coil broadband transformer, exhibiting high even-mode rejection, provides the balanced drive for the local oscillator excitation of the quad FET gates. The gates of the quad array have very low conductance; hence there will be some degree of mismatch to the local oscillator, which normally could not be tolerated for the signal port. The high gate impedance, however, allows a moderate level of local oscillator power to bring about the necessary gate voltage swing.

Transformer Design

The design problems encountered in a single-balanced mixer are compounded in the double-balanced mixer: the full-wave JFET quad differs markedly from the half-wave single-balance JFET pair, in that the quad is represented as a 4-terminal input structure, while the JFET pair is represented as a 2-terminal structure. Consequently, the double-balanced mixer transformer design requires two separate solutions, each offering entirely different structures. While each transformer design will be treated separately, it is important to note the design goals which are common to both.

The transformers must:

1. Consist of three single-ended terminal pairs, an input and a balanced output;
2. Offer a broadband match between the unbalanced input and a symmetrical balanced load;
3. Maintain (over a wide bandwidth) a differential phase of 180° across the symmetrical balanced loads; and
4. Introduce a minimum of insertion loss.

Signal Input Transformer Design

In general, design and fabrication of broadband transformers has been limited to the popular ferrite-core varieties derived from transmission-line theory[11], where exceptional bandwidths are possible. The more popular transformer designs frequently result in a 4:1 impedance transformation, as in the single-balanced mixer or in most trifilar designs. Other popular transformers offer either simple constant-impedance phase inversion or unbalanced-to-balanced configurations.

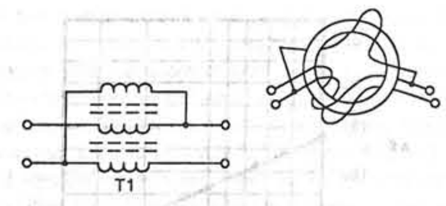

Figure 18. Signal Input Transformer

The JFET quad signal input terminals consists of shunt pairs of JFET source terminals which offer a combined load impedance of about 35 Ω as contrasted to a 100 Ω impedance value which would have suited a 4:1 transformer. It was thus necessary to design a broadband unbalanced-to-split-balance transformer which produced, in effect, a 50 Ω asymmetrical input to a 25-0-25 Ω output.

Such a transformer would require an unbalanced 50 Ω input and a symmetrically-balanced output having near-perfect 180° phase differential and an equipotential, (even-mode) center tap. Consequently, a two-step design procedure was indicated.

The first step was to design a transformer which would provide the unbalanced-to-balanced transition while maintaining a constant impedance of 50 Ω and a 180° phase differential across the balanced output, over a 50-250 MHz band. The design was straightforward, and is shown schematically in Figure 18. The extra winding was required to complete the necessary magnetization current path.

Design of the core windings required selection of the proper ferrite, and establishment of the actual winding length. The latter was resolved to a first-order approximation by the formulas of Pitzalis (Equations 19 and 20).

Having established the approximate length limits, the final solution came by experiment. A Hewlett-Packard 8405A vector voltmeter was invaluable during this phase of the work.

According to Ruthroff the simple balun, to which the signal input transformer can be most readily compared, is equivalent to "an ideal reversing transformer plus a length of transmission line. If the characteristic impedance of the line is equal to the terminating impedance, the transformer is inherently broadband." The true equivalent of the simple Ruthroff balun is shown in Figure 19, where the "length of transmission line" is in effect a shunt element of characteristic admittance, Y_s. If $Y_o = Y_{in} = Y_A$, then it can be shown that $Y_s = Y_A$, thus providing a flat admittance transfer through the transformer[12]. Construction of the "ideal reversing transformer" required three turns-per-inch of Belden #24 enamel wire for a characteristic admittance of 0.22 ℧.

Core permeability was established by selection from three possible choices of Indiana General ferrite (Q1 for a permeability, μ/μ_o of 125; Q2 for $\mu/\mu_o = 40$; and Q3 for $\mu/\mu_o = 16$). Figure 20a provides a performance comparison between identically-wound transformers with different core permeabilities; Figure 20b shows the effects of winding length on the selected core, Q2. (Core material Q3 might have offered a better permeability, but its cost was prohibitive). A winding length of 1.5 inches was used for this first-stage transformer design. An identical length of single conductor was wound about the core in the

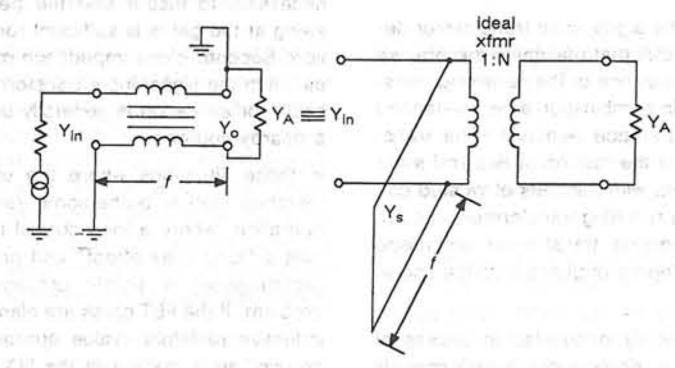

Figure 19. Equivalence of Simple Balun

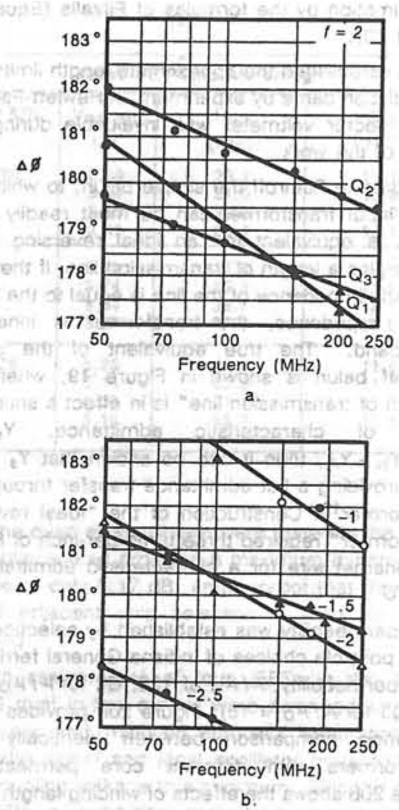

Figure 20. Differences in Core Permeability

same winding direction for the magnetization requirements.

The second phase of the signal input transformer design is to provide a circuit that maintains the precise impedance and phase balance of the reversing transformer, while offering in combination a center-tapped junction with high even-mode rejection. The transformer was wound after the fashion of Ruthroff's 4:1 ratio impedance design, with 2 inches of twisted pair wire on a Q2 core. The resulting transformer, in combination with the reversing transformer discussed earlier, provided the degree of phase balance shown in Figure 21.

The center tap is typically decoupled in excess of 50 dB. The completed signal input transformer is shown in Figure 22. If the design offers the assurance

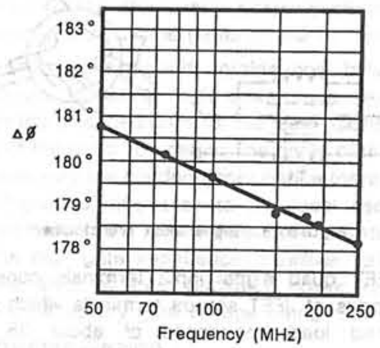

Figure 21. Input Transformer Phase Balance

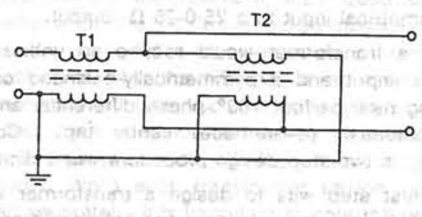

Figure 22. Completed Signal Input Transformer

that the center tap will be grounded, then the magnetization winding may be omitted.

Local Oscillator Input Transformer

Design of the local oscillator transformer is somewhat simpler than that of the signal input transformer, because two design rules may be relaxed. First, the gates operate at a higher impedance than that imposed on the sources; thus it is only necessary to insure that the peak-to-peak voltage swing at the gates is sufficient for proper FET operation. Second, close impedance match is not so critical as in the signal input transformer, since the local oscillator excitation is generally derived directly from a nearby source.

In those situations where the existence of a mismatched load is bothersome (as in high-frequency operation, where a long coaxial feed will tend to exhibit a "long lines effect" and produce erratic mixer performance) a simple precaution will avoid the problem. If the FET gates are clamped with fixed non-inductive resistors (value approximately 200 Ω) to ground, such loading of the LO transformer secondary will insure a reasonable input match.

In the design shown in Figure 23, a simple trifilar-wound toroidal-core transformer produced excellent results. The transformer was constructed from three strands of Belden #24 enamel wire, twisted to 3 turns per inch. The trifilar winding, 2 inches long, was wrapped around an Indiana General F625-9 (CF102) Q2 toroidal core. Care must be taken when winding multifilar transformers with heavy wire, to insure that the wire is wrapped tightly around the ferrite for good even-mode isolation and balance.

Simplicity of design of the combined transformers made detailed analysis of performance unnecessary; indicators such as isolation and dynamic unbalance are sufficient to show symmetry for both transformers and the FET quad.

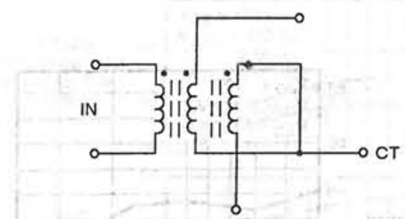

Figure 23. Local Oscillator Input Transformer

(For the prototype mixer feasibility study, relatively large ferrite cores were used, as a matter of winding convenience. The practice of using large cores, however, can lead to excessive transformer losses, resulting in degraded mixer efficiency, high noise figures, high LO drive requirements and reduced gain. For best results, cores no larger than those commonly used in the CATV industry should be chosen).

AM Local Oscillator Noise Rejection

Originally, balanced mixers were used for the specific purpose of canceling spurious AM signals existing on or about the local oscillator carrier (the function of the mixer in establishing good inter-port isolation was a side-effect). These signals could be either spurious AM signals generated on or about the carrier (Figure 24) or actual signals existing at the signal frequency. In the latter case, the signals enter the mixer through the local oscillator, having found their way in through some leakage coupling phenomenon.

Regardless of the type or source of AM signals entering through the local oscillator port, the balanced mixer should effectively reject these signals so that

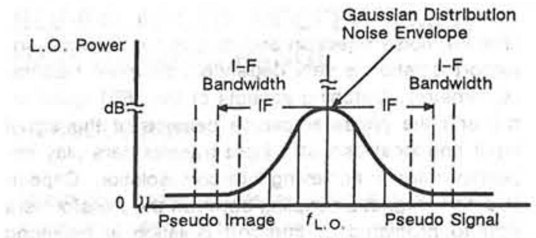

Figure 24. Generation of Spurious AM Signals

their products do not occur at the intermediate frequency. In the early days of balanced mixers, a 20 dB rejection of AM noise was considered good; today's sophisticated techniques for selection of dynamically-matched semiconductors can provide ultimate AM rejection in excess of 30 dB. Figure 25 provides an insight into the degree of AM noise rejection available in the double-balanced mixer.

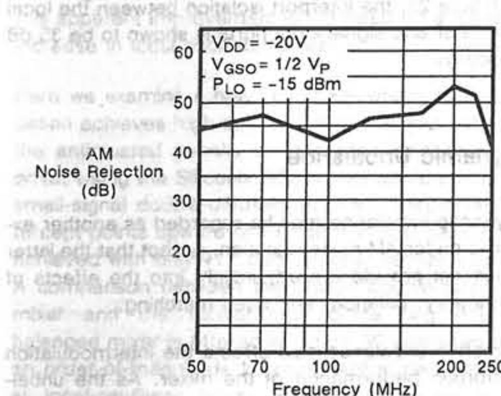

Figure 25. AM Noise Rejection in Double-Balance Mixer

(Insofar as FM noise is concerned, it should be noted that no mixer is capable of rejecting frequency-modulated signals entering through the local oscillator).

An interesting point not generally considered in discussions of balanced mixers is that the dynamic range of the mixer can be limited by the conversion of local oscillator *noise* into the intermediate frequency, which tends to blank out a weak signal and place a bottom on sensitivity.

Interport Isolation

Like AM noise rejection and dynamic unbalance, interport isolation is very dependent on mixer balance (symmetry). Matching aspects of the JFET quad array and the phase/amplitude balance of the signal input and local oscillator input transformers play important roles in achieving interport isolation. Capacitive and magnetic coupling between the transformers add to problems of interport isolation in balanced mixers.

(In the prototype mixer, the JFET quad was packaged in a 14-pin dual in-line housing, as a matter of construction convenience.) The U350 is recommended for double-balanced mixer designs.

Interport isolation was also enhanced in the prototype mixer through careful parts layout. As a measure of the overall effects of unbalance, a quantitative measurement of interport isolation vs dynamic unbalance is made in Figure 26.

In Figure 27, the interport isolation between the local oscillator and signal input ports is shown to be 35 dB typically.

Dynamic Unbalance

Dynamic unbalance may be regarded as another expression for AM noise rejection, except that the latter does not provide a ready insight into the effects of symmetry, balance, and quad matching.

Dynamic unbalance also affects the intermodulation distortion performance of the mixer. As the unbalance approaches a degree of true balance, the IMD tends to optimize; conversely, when unbalance is excessive the IMD approaches an asymptotic state. This effect is shown in Figure 28.

Designing the IF Network

The IF network performs three important functions in the FET double-balanced mixer. As with the single-balanced mixer, it provides for best match between the quad FETs and the intermediate frequency amplifier; it effectively bypasses the RF components (signal and local oscillator); and unique to the double-balanced mixer, it provides a reduction of simple harmonic distortion, by virtue of its balance.

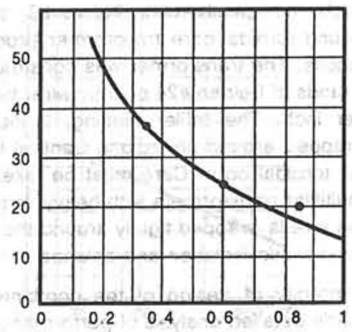

Figure 26. AM Noise Rejection in Double-Balance Mixer

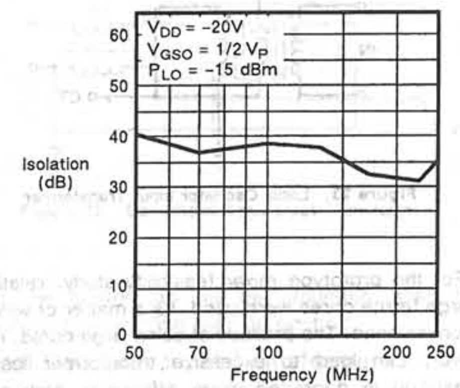

Figure 27. Interport Isolation

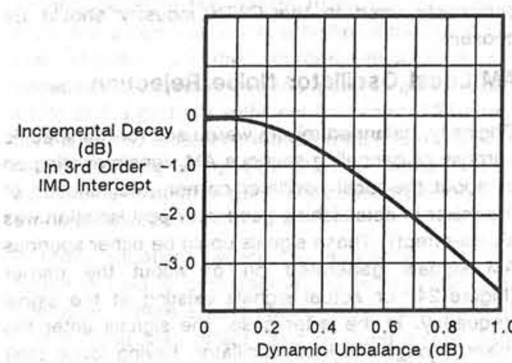

Figure 28. Dynamic Unbalance vs. Incremental Decay

Selection of the dynamic drain impedance value in the IF network is a critical point in the design of the structure. Both IM product distortion and cross-modulation will be affected by the instantaneous peak-to-peak voltage of the FETs if the dynamic drain impedance allows the signal peaks to enter either the pinchoff or breakdown voltage regions of the transistors. Here another design tradeoff must be considered. If the impedance is too high, the dynamic range of the mixer will be limited; if the impedance is too low, useful conversion gain will be sacrificed, as shown in Figure 29.

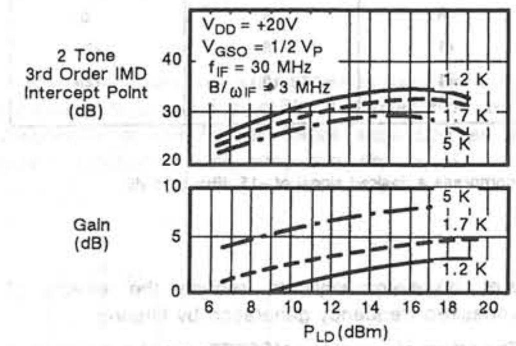

Figure 29. Gain and IMD vs. Local Oscillator Drive

Mixer Performance

Quad FET arrays with both high and low pinchoff voltage levels were used in evaluation of the active double-balanced mixer; the prototype mixer exhibited clearly superior characteristics, compared to equivalent low-small-signal passive double-balanced mixers. The low- to medium-level pinchoff voltage quad FET array performed slightly better than the high-level pinchoff devices (5.5 V), solely because of a limitation in available local oscillator power. Performance of several types of mixers is made in Table 8.

Conclusion

It may be concluded that performance of the active double-balanced mixer contributes overall system gain in areas critical to telecommunications practice, and reduces associated amplifier requirements.

SECTION 3: A COMMUTATION DOUBLE-BALANCED MOSFET MIXER OF HIGH DYNAMIC RANGE

INTRODUCTION

Heretofore, most mixers sporting a high dynamic range have been either the passive diode-ring variety - available from numerous vendors - or the active FET mixer. The latter is often implemented, using either the Siliconix U310 or the Siliconix U350, as described in Sections 1 and 2.

Common to both the diode and FET is their square-law characteristic so important in maintaining low distortion during mixing. However, equally important for high dynamic range is the ability to withstand overload that has been identified as a principle cause of distortion in mixing[13]. Some passive diode-ring mixer designs have resorted to paralleling of diodes to effect greater current handling, yet the penalty for this apparent improvement is the need for a massive increase in local-oscillator power.

Here we examine a new FET mixer where communication achieves high dynamic range without exacting the anticipated penalty of increased local-oscillator drive. Using the Siliconix Si8901 monolithic quad-ring small-signal double-diffused MOSFET, third-order intercept points upward of +39 dBm (input) have been achieved with only +17 dBm of local-oscillator drive. A comparison between the Si8901 double-balanced mixer and the conventional diode ring double-balanced mixer is offered in Figure 30 where we see an order-of-magnitude improvement in performance at local-oscillator power levels substantially lower than heretofore possible with the conventional mixer.

Conversion Efficiency Of The Commutation Mixer

Unlike either the conventional diode-ring mixer or the active FET mixer, the commutation mixer relies on the switching action of the quad-FET elements to effect mixing action. Consequently, the commutation mixer is, in effect, no more than a pair of switches reversing the phase of the signal carrier at a rate determined by the local-oscillator frequency. Ideally, we would anticipate little noise contribution, and

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Table 8
Comparison Between Active, Passive, and MOSFET Double-Balanced Mixers

Characteristic	Active FET	Passive Low-Level	Passive High-Level	MOSFET Switch
Frequency Range (MHz)	50-250	0.5-500	0.5-500	0.2-100
AM Local Oscillator Noise Rejection (dB)	45	Unknown	Unknown	Unknown
Dynamic Unbalance (dB)	0.15	Unknown	Unknown	Unknown
Isolation RF-Local Oscillator (dB)	35	35	40	30
Isolation Local Oscillator - RF (dB)	60	25	30	25
Overall Noise Figure (SSB) (dB)	8.0	8.5	8.5	9.0
Local Oscillator Drive Level (dBm)	+15	+7	+17	+30
Two-Tone IMD Intercept Point* (dBm)	+34	+15	+28	35
Conversion Gain (db)	+4	-8	-8	-8
1 dB Compression (dBm)	+13	+1	+8	+29
Desensitization Level** (dBm)	+13	+1	+8	+29

* Output - measured at recommended LO drive level.

** The level for a nearby unwanted signal (separated 200 kHz) to compress a desired signal of –15 dBm by 1 dB.

since the switching mixer - consisting of four MOSFET "switches" - has finite ON-state resistance, performance is similar to that of a switching attenuator. As a result, the conversion efficiency of the commutation mixer may be expressed as a loss.

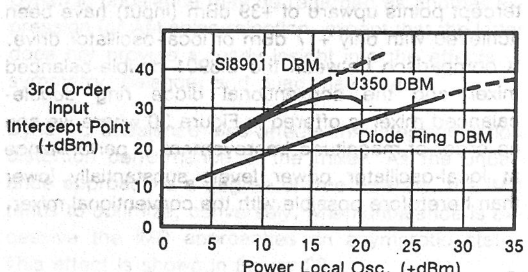

Figure 30. Performance Comparison of Double Balanced Mixers

This loss results from two related factors. First, is the r_{DS} of the MOSFET relative to the signal impedance (R_g) and intermediate frequency (IF) impedance (R_L); second - and a more common and expected factor - is the loss attributed to signal conversion to undesired frequencies. The latter signal conversion involves the image and harmonic frequencies. There are, however, ways to reduce the effects of undesired frequency generation by filtering.

The effect of r_{DS} of the MOSFETs may be determined from the analysis of the equivalent circuit shown in Figure 31, assuming that our local oscillator wave form is an idealized square wave. It is not, but if we assume that it is, our analysis is greatly simplified; and for a commutation mixer, a high local-oscillator voltage begins to approach the ideal waveform of a square wave.

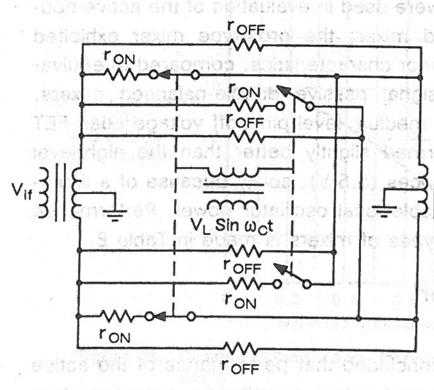

Figure 31. Equivalent Circuit of Communication Mixer

Figure 31, showing switches rather than MOSFETs, also identifies the ON-state resistance, r_{DS}, as well as the OFF-state resistance, r_{OFF}. The latter can be disregarded in this analysis as it is generally extremely high ($2 \bullet 10^9\ \Omega$). On the other hand, the ON-state resistance, r_{DS}, together with the source and load impedances (i.e. signal and intermediate-frequence impedances) directly affects the conversion efficiency.

If we assume that our local-oscillator excitation is an idealized square wave, the switching action may be represented by the Fourier series as,

$$f(x) = \frac{1}{2} + \frac{2}{\pi} \sum_{n=1}^{\infty} \frac{\sin(2n-1)\,\omega t}{(2n-1)} \qquad (25)$$

The switching function, $\epsilon(t)$, shown in the derivative equivalent circuit of Figure 32, is derived from the magnitude of this Fourier series expansion as a *power* function by squaring the first term, i.e. $(2/\pi)^2$.

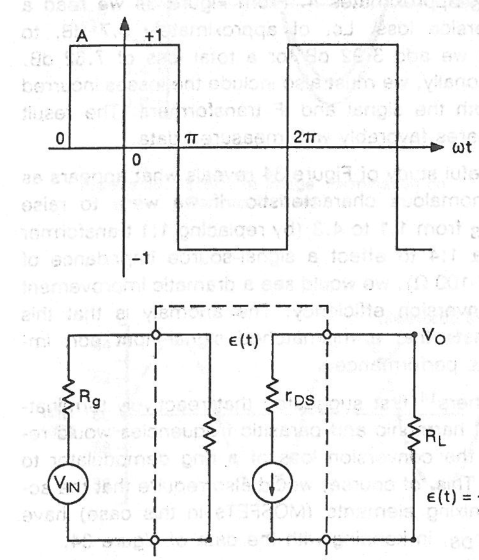

Figure 32. Derivative Equivalent Circuit

The available power that can be delivered from a generator of RMS open-circuit terminal voltage, V_{IN}, and internal resistance, R_g, is

$$P_{av} = \frac{V_{IN}^2}{4 R_g} \qquad (26)$$

or, in terms shown in Figure 33

$$P_{av} = \frac{V_{IN}^2}{\pi^2 R_g} \qquad (27)$$

the output power, deliverable to the intermediate-frequency port, is

$$P_{out} = \frac{V_O^2}{R_L} \qquad (28)$$

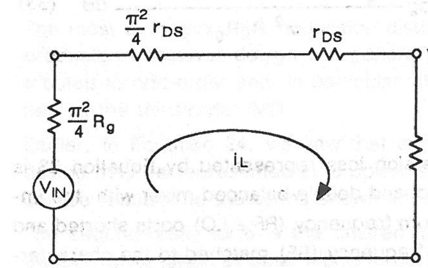

Figure 33. The Power-Loop Circuit with All Elements Equivalent Based on the Transfer Function, $\epsilon(t) = \frac{4}{\pi^2}$

To arrive at V_o, we first need to obtain the loop current, i_L, which from Figure 33 offers

$$i_L = \frac{V_{in}}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad (29)$$

then

$$V_O = \frac{V_{in} R_L}{\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}} \qquad (30)$$

Combining Equations 28 and 30,

$$P_{out} = \frac{V_{in}^2 R_L}{\left[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}\right]^2} \qquad (31)$$

Conversion efficiency - in the case for the commutation mixer, a loss - may be calculated from the ratio of P_{av} and P_{out}

$$L_C = 10 \text{ Log } \frac{P_{av}}{P_{out}} \text{ dB} \tag{32}$$

Substituting Equation 27 for P_{av}, and Equation 31 for P_{out}, we obtain

$$L_C = 10 \text{ Log } \frac{\left[\frac{\pi^2}{4}(R_g + r_{DS}) + R_L + r_{DS}\right]^2}{\pi^2 R_L R_g} \text{ dB} \tag{33}$$

The conversion loss represented by Equation 33 is for a broadband double-balanced mixer with the image and sum frequency (RF + LO) ports shorted and the signal frequency (RF) matched to the characteristic line impedance. The ideal commutating mixer operating with resistive source and load impedances will result in having the image and all harmonic frequencies dissipated. For this case, the optimum conversion loss reduces to

$$L_C = 10 \text{ Log } \frac{\pi^2}{4} \text{ dB} \tag{34}$$

or -3.92 dB

However, a truly optimum mixer also demands that the MOSFETs exhibit an ON-state resistance of zero ohms and, of course, an ideal square-wave excitation. Neither is possible in a practical sense.

Equation 33 can be examined for various values of source and load impedances as well as r_{DS} by graphical representation, as shown in Figure 34, remembering that a nominal 3.92 dB must be added to the values obtained from the graph.

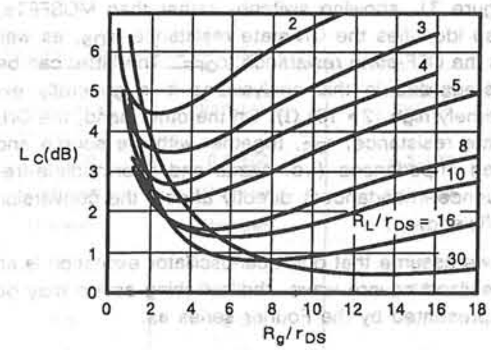

Figure 34. Insertion Loss As A Function of r_{DS}, R_L & R_g

To illustrate how seriously the ON-state resistance of the MOSFETs affects performance, we need only to consider the Si8901 with a nominal r_{DS} (at V_{GS} = 15V) of 23 Ω. With a 1:1 signal transformer (50 to 25-0-25 Ω), R_g/r_{DS} = 1.1. Allowing a 4:1 IF output transformer to a 50-Ω preamplifier, the ratio R_L/r_{DS} approximates 4. From Figure 34 we read a conversion loss, Lc, of approximately 3.7 dB, to which we add 3.92 dB for a total loss of 7.62 dB. Additionally, we must also include the losses incurred by both the signal and IF transformers. The result compares favorably with measured data.

A careful study of Figure 34 reveals what appears as an anomalous characteristic. If we were to raise R_g/r_{DS} from 1.1 to 4.3 (by replacing 1:1 transformer with a 1:4 to effect a signal-source impedance of 100-0-100 Ω), we would see a dramatic improvement in conversion efficiency. The anomaly is that this suggests that a mismatched signal-input port improves performance.

Caruthers[14] first suggested that reactively terminating all harmonic and parasitic frequencies would reduce the conversion loss of a ring demodulator to zero. This, of course, would also require that the active mixing elements (MOSFETs in this case) have zero r_{DS}, in keeping with the data of Figure 34.

A double-balanced mixer is a 4-port - consisting of a signal, image, IF, and a local-oscillator port. Of these, the most difficult to terminate is the image frequency port simply because, in theory, it exists as a separate port, but in practice it shares the signal port. Any reactive termination would, therefore, be narrow-band irrespective of its proximity to the active mixing elements.

The performance of an image-termination filter offering a true reactance to the image frequency (100% reflective) may be deduced to a reasonable degree from Figure 34, if we first presume that the conversion loss between signal and IF compares with that between signal and image. The relationship is displayed in Figure 35 where we see the expected variation in amplitude proportional to conversion efficiency (inversely proportional to conversion loss).

Image-frequency filtering affects more than conversion efficiency. As the phase of the detuned-short position of the image-frequency filter is varied, we are able to witness a cyclical variation in the intermodulation distortion as has been confirmed by measurement, shown in Figure 36. By comparing Figure 35 with Figure 36, we see that any improvement in conversion loss appears to offer a corresponding degradation in intermodulation distortion!

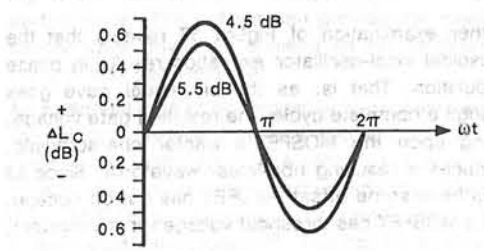

Figure 35. Effect of Image Termination on Conversion Loss

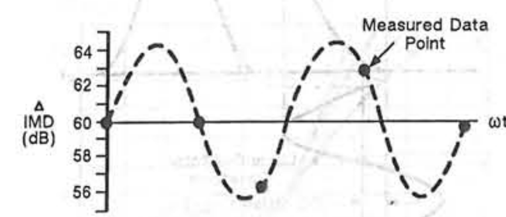

Figure 36. Effect of Image Termination on 3rd-Order Distortion

Intermodulation Distortion

Unbalanced, single-balanced, and double-balanced mixers are distinguished by their ability to selectively reject spurious frequency components, as defined in Table 5. The double-balanced mixer, by virtue of its symmetry, suppresses twice the number of spurious frequencies as the single-balanced mixer suppresses.

In the ideal mixer, the input signal is translated to an intermediate frequency without distortion, that is without imparing any of the contained information. Regrettably, the ideal mixer does not occur in practice. Because of certain non-linearities within the switching elements (MOSFETs in this case) as well as imperfect switching resulting in phase modulation, distortion results.

Identifying Intermodulation Distortion Products

The most damaging intermodulation distortion (IMD) products in receiver design are generally those attributed to odd-order and, in particular, those identified as the third-order IMD.

Earlier, in Equation 24, we saw that any non-linear device may be represented as a power series which can be reduced to the terms shown in Table 6.

The second-order term is the desired intermediate frequency we seek, all other higher-orders are undesirable but, unfortunately, are present to a varying degree.

There are both fixed-level IMD products and level-dependent IMD products. The former are produced by the interaction between a fixed-level signal, such as the local oscillator and the variable-amplitude signal. The resulting frequencies may be identified by

$$n f_1 \pm f_2 \tag{35}$$

where, n is an integer greater than 1.

Level-dependent IMD products result from the interaction of the harmonics of the local oscillator and those of the signal. The resulting frequencies may be identified by

$$n f_1 \pm m f_2 \tag{36}$$

where, m and n are integers greater than 1.

For a mixer to generate IMD products at the intermediate frequency, we must account for at least a two-step process. First, the generation of the harmonics of the signal and local oscillator; and second, the mixing or conversion of these frequencies to the intermediate frequency. Consequently, the mixer may be modeled as a series connection of two non-linear impedances, the first to generate the harmonic products and the second to mix or convert to the intermediate frequency. Although many harmonically-related products are possible, we will focus principally on the odd-order IMD products.

If we allow two interfering signals, f1 and f2, to impinge upon the first non-linear element of our mixer model, the result will be 2f1 - f2 and 2f2 - f1. These are identified as third-order intermodulation products (IMD_3). Other products are also generated taking the form 3f1 - 2f2 and 3f2 - 2f1, called fifth-order IMD products (IMD_5). Unlike the even-order products, odd order products lie close the the fundamental signals and, as a consequence, are most susceptible to falling within the passband of the intermediate frequency and thus degrading the performance of the mixer.

A qualitative definition of linearity based upon intermodulation distortion performance is called the intercept point. Convergence occurs when

- the fundamental output (IF) response is directly proportional to the signal input level;
- the second-order output response is proportional to the square of the signal input level; and,
- the third-order output response is proportional to the cube of the signal input level.

The point of convergence is termed the intercept point. The higher the value of this intercept point, the better the dynamic range.

Intermodulation Distortion in the Commutation Mixer

Although the double-balanced mixer outperforms the single-balanced mixer as we saw in Table 5, a more serious source of intermodulation products results when the local-oscillator excitation departs from the idealized square wave[15,16]. This phenomena is easily recognized by a careful examination of Figure 37, where a sinusoidal local-oscillator voltage reacts not only upon a varying transfer characteristic but also on a varying non-linear, voltage-dependent capacitance (not shown in Figure 37). Although the effects of this sinusoidal transition are not easily derived, Ward[17] and Rafuse[18] have concluded that lowering R_g will provide improved intermodulation performance! This conflicts with low conversion loss, as we saw in Figure 34, but agrees with Equation 37.

$$20 \text{ Log} \left(\frac{V_S}{\frac{t_r\, \omega_{LO}\, V_C}{8}}\right)^2 \text{dB} \qquad (37)$$

where,

V_C is the peak-to-peak local-oscillator voltage,

V_S is the peak signal voltage,

t_r is the rise and fall time of V_C,

ω_{LO} is the local-oscillator frequency.

Further examination of Figure 37 reveals that the sinusoidal local-oscillator excitation results in phase modulation. That is, as the sinusoidal wave goes through a complete cycle, the resulting gate voltage, acting upon the MOSFET's tranfer characteristic, produces a resulting non-linear waveform. Since all FETs have some offset - a JFET has cut-off voltage, and a MOSFET has threshold voltage - it is important,

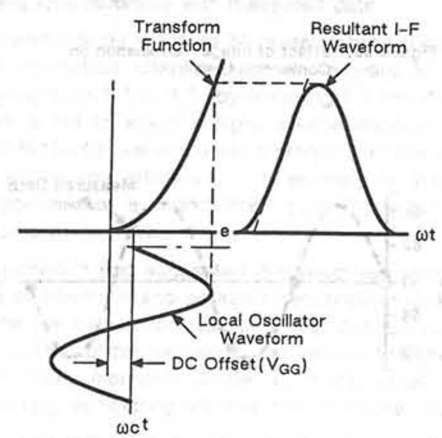

Figure 37. Effect of Sinusoidal L.O. Waveform on I-F Linearity

both for symmetry as well as for balance, to offer some dc offset voltage to the gates. Optimum IMD performance demands that the switches operate in a 50% duty cycle; that is, the switches must be fully ON and fully OFF for equal time. Without some form of offset bias, this would be extremely difficult unless we were to implement an idealized square-wave drive.

Walker[19] has derived an expression showing the predicted improvement in the relative level of two-tone third-order intermodulation products (IMD_3) as a function of the rise and fall times of the local-oscillator waveform.

Equation 37 offers us several interesting aspects on performance. Since any reduction in the magnitude of V_S improves the IMD, we again discover that by lowering R_g (which, in turn, decreases the magnitude of V_S) appears to benefit performance. Second, the higher the local-oscillator voltage, the better the IMD performance. Third, if we can provide the idealized square-wave drive, we achieve an infinite improvement in IMD performance!

An additional fault of sinusoidal local-oscilaltor excitation results whenever the wave approaches the zero-crossing at half-period intervals. As the voltage decays, we find that any signal voltage may overload the MOSFETs causing intermodulation and crossmodulation distortion[20]. This can be easily visualized from Figure 38 where we see the classic i-e characteristics of the MOSFET at varying gate voltages. Only at substantial gate voltage do we witness reasonable linearity and, consequently, good dynamic range.

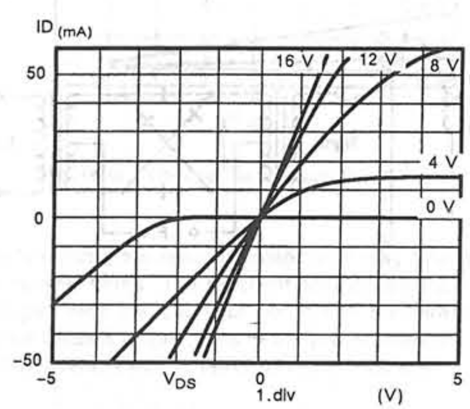

Figure 38. First & Third Quadrant I-E Characteristics Showing Effect of Gate Voltage Leading to Large-Signal Overload Distortion

Dynamic Range Of The Commutation Mixer

As the two-tone intercept point increases in magnitude, we generally expect a like improvement in dynamic range results. Yet, as we have concluded from earlier study, the intermodulation products appear to be a function of both the generator or source impedance as well as ratio R_g/r_{DS} and R_L/r_{DS} (Figure 34).

In any receiver, performance can be quantified by the term *dynamic range*. Dynamic range can be extended by improving the sensitivity to low-level signals and by increasing the power handling ability without being overcome by interfering intermodulation products or the effects caused from desensitization.

There are rules to follow if we are to improve the low-level signal sensitivity. Ideally we would like a mixer to be transparent, acting only to manipulate the incoming signals for easy processing by subsequent equipment. The perfect mixer would have no conversion loss and a low noise figure. However, in the preceding analysis we discovered that optimum intermodulation performance occurred when the signal input port is mismatched to the quad MOSFETs (Figure 34). It now becomes clear that a performance trade-off appears necessary. Either we seek low conversion loss and with it a higher noise figure, or we aim for the highest two-tone third-order intercept point. Fortunately, as we seek the latter, our dynamic range will actually improve since a mismatched signal port has less effect upon the signal-to-noise performance of the mixer than does a matched signal port have upon intermodulation distortion.

Convention has identified minimum sensitivity to be the weaker signal which will produce an output signal that is 10 dB over that of the noise in a prescribed bandwidth (usually 1kHz), or

$$\text{Sens.} = 20 \text{ Log} \frac{V_S + V_N}{V_N} + \text{dB} \qquad (38)$$

Desensitization occurs whenever a nearby unwanted signal causes the compression of the desired signal. The effect appears as an increase in the mixer's conversion loss.

9

The Si8901 As A Commutation Mixer

Because of package and parasitic constraints, the Si8901 is best suited for performance in the HF to low VHF region. A surface-mount version may extend performance to somewhat higher frequencies.

In our review of intermodulation distortion, we recognized that to achieve a high intercept point the local-oscillator drive must

- approach the ideal square-wave,
- ensure a 50% duty cycle,
- offer sufficient amplitude to ensure a full ON and OFF switching condition, as well as to offer reduced r_{DS} when ON.

Furthermore, to maintain superior overall performance - both in conversion loss, dynamic range (noise figure) and intercept point - some form of image-frequency termination would be highly desirable even though, understandably, the mixer's bandwidth would be restricted.

Consequently, the principal effort in the design of a high dynamic range commutation mixer is two-fold. First, and most crucial, is to achieve a gating or control voltage sufficient to ensure a positive and hard turn-ON as well as a complete turn-OFF of the mixing elements (MOSFETs). Second, and of lesser importance, is to properly terminate the parasitic and harmonic frequencies developed by the mixer.

Establishing the Gating Voltage

Local oscillator injection to the conventional diode ring, FET, or MOSFET double-balanced mixer is by the use of the broadband, transmission-line transformer, as shown in Figure 39. For the diode-ring mixer where switching is a function of loop current, or for active FET mixers that operate on the principle of transconductance and thus need little gate voltage, the broadband transformer is adequate. If this approach is used for the commutation mixer, we would need extraordinarily high local-oscillator drive to ensure positive turn-ON. Rafuse and Ward used a minimum of 2 W to ensure mixing action; Lewis and Palmer achieved high dynamic range using 5 Watts! The MOSFETs used in these early designs were p-channel, enhancement-mode (2N4268 devices with moderately high threshold (6 V maximum) and high input capacity (6 pF maximum). All of these early MOSFET double-balanced mixers relied on the conventional 50 to 100-0-100 Ω transformer for local-oscillator injection to the gates.

A major goal is the conservation of power. This goal cannot be achieved using the conventional design. Simply increasing the turns ratio of the coupling transformer is thwarted by the reactive load presented by the gates.

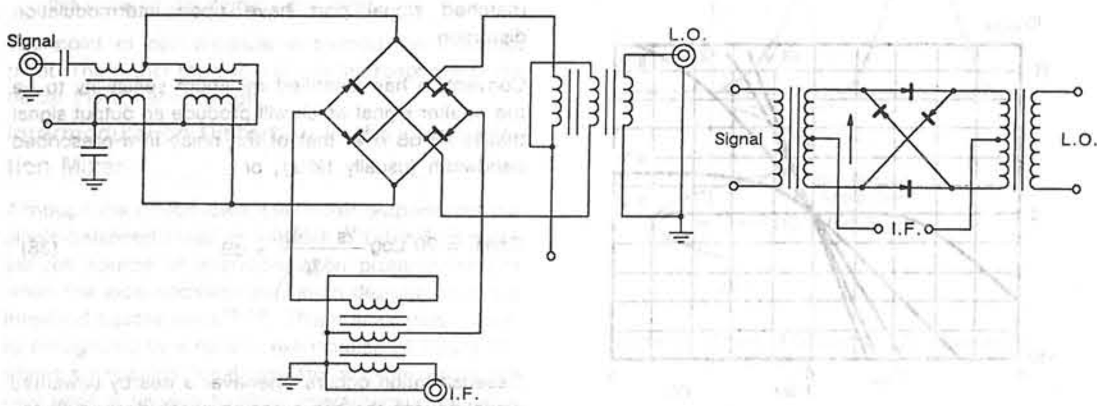

Figure 39. Local Oscillator Drive Using Conventional Broadband Transformers

The obvious solution is to use a resonant gate drive. The voltage appearing across the resonant task - and thus on the gates - may easily be calculated.

$$V = (P \bullet Q \bullet X)^{1/2} \qquad (39)$$

Where, P is the power delivered to the resonant tank circuit,

Q is the loaded Q of the tank circuit, and

X is the reactance of the gate capacity.

Since the gate capacitance of the MOSFET is voltage dependent, the reactance of the gate becomes dependent upon the impressed excitation voltage. To allow this would severely degrade the IMD performance of the mixer. However, we can minimize the change in gate capacitance and remove its detrimental influence using a combination of substrate and gate bias, as shown in Figure 40. Not only does this show itself beneficial in this regard, but as we saw in Figure 37, a gate bias is necessary to ensure the required 50% duty cycle. Furthermore, a negative substrate voltage ensures that each MOSFET on the monolithic substrate is electrically isolated and that each source-/drain-to-body diode is sufficiently reverse biased to prevent half-wave conduction.

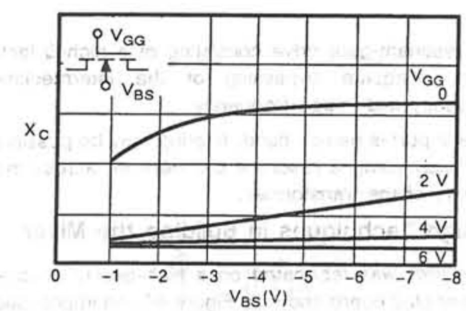

Figure 40. Effect of Bias on Gate Reactance

Implementing the resonant gate drive may take any of several forms. The resonant tank circuit may be merged with the oscillator, or it can be varactor-tuned Class B stage, or as in the present design, an independent resonant tank, shown in Figure 41.

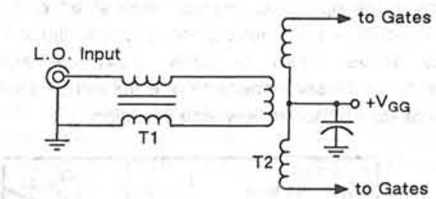

Figure 41. Resonant - Gate Drive. T2 is Tuned to Resonate with C_{gs} of Si8901

To ensure symmetrical gate voltage in 180-degree anti-phase, if the local-oscillator drive is asymmetrical, i.e., fed by unbalanced coax, an unbalanced-to-balanced balun must be used (T1 in Figure 41); otherwise, capacitive unbalance results with an attendant loss in mixer performance.

Table 9 offers an interesting comparison between a resonant-gate drive with a loaded tank Q of 14 and a conventional gate drive using a 50 to 100-0-100 Ω transformer. The importance of a high tank Q is graphically portrayed in Figure 42. The full impact of a high gate voltage swing can be appreciated by using Equation 37. Here, as V_C (gate voltage) increases the intermodulation performance (IMD) also improves, as we might intuitively expect. Calculated and measured results are shown in Figure 43 and demonstrate reasonable agreement. The difference may reflect problems encountered in measuring V_C as any probe will inadvertently load, or detune, the resonant tank even with the special care that was taken to compensate.

Table 9

Power in (mW)	NR Gate Voltage (V)	Res Gate Voltage (V)
10	0.20	5.4
20	0.29	7.7
30	0.33	9.4
60	0.44	13.3

Comparison of a-c gate voltage versus local-oscillator drive between a non-resonant (NR) and resonant (Res) tank with a loaded Q of 14 (Freq. 150 MHz)

If we have the option to choose "high side" or "low side" injection - i.e., having the local-oscillator frequency above (high) or below (low) the signal frequency - a closer inspection of Equation 37 should convince us to choose low-side injection.

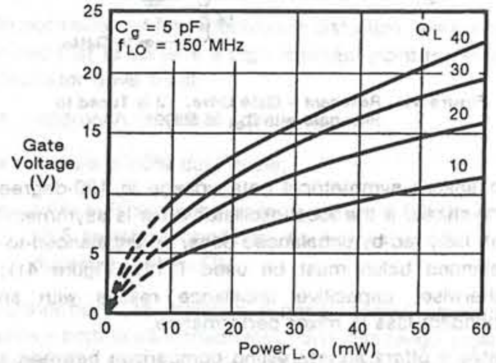

Figure 42. Influence of Loaded Q on Gate Voltage vs. L.O. Power

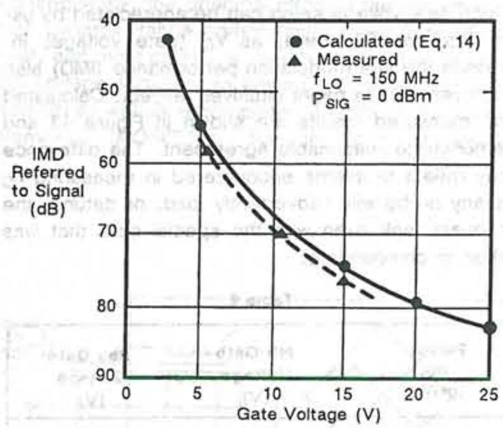

Figure 43. Effect of Gate Voltage on IMD Performance

Terminating Unwanted Frequencies

If our mixer is to be operated over a restricted frequency range where the local oscillator and signal frequencies can be manipulated, image-frequency filtering may be possible. Image-frequency filtering does affect performance - for high-side local-oscillator injection, an elliptic-function low-pass filter, or for low-side injection, a high-pass filter might offer worthwhile improvement. In either case, the filter offers a short-circuit reactance to the image frequency forcing the image to return once again for demodulation. The results of using a low-pass filter with the prototype commutation mixer are known from our earlier examination of Figures 35 and 36.

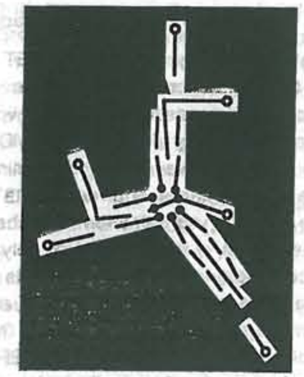

Figure 44. Mask Layout PCM Prototype Commutation Mixer

The resonant-gate drive consisting of a high-Q tank offers adequate bypassing of the intermediate frequency and image frequency.

If the IF port is narrow band, filtering may be possible by simply using a resonant L-C network across the primary of the transformer.

Design Techniques in Building the Mixer

The mixer was fabricated on a high-quality double-copper clad board shown in Figure 44. An improvised socket held the Si8901.

The signal and IF ports used Mini-Circuits, Inc., plastic T-case RF transformers. For the intermediate frequency, the Mini-Circuits T4-1 (1:4) was used; for the signal, the Mini-Circuits T1-1T (1:1) was used. The resonant tank was wound on a one-quarter-inch-diameter ceramic form with no slug. The unbalanced-to-balanced resonant tank drive used a T4-1. The schematic diagram, Figure 45, is for a commutation mixer, operating with an IF of 60 MHz.

The principle effort involved the design of the resonant-gate drive. This necessitated an accurate knowledge of the gate's total capacitive loading effect. To accomplish this, a precision fixed capacitor (5 pF) was substituted for the Si8901, and at resonance, it was a simple matter to calculate the inductance of the resonant tank. Substituting the Si8901 made it again a simple task to determine the capacitive effects of the Si8901. Once known, a high-Q resonant tank can be quickly designed and implemented. To ensure good interport isolation, symmetry is important, so care is necessary in assembly to maintain mechanical symmetry, especially with the primary winding.

Performance of the Si8901 Prototype Commutation Mixer

The primary goal in developing a commutation double-balanced mixer is to achieve a wide dynamic range. If this task can be accomplished with an attendant savings in power consumption, then the resulting mixer design should find wide application in HF receiver design.

The following tests were performed.

- conversion efficiency (loss)
- two-tone, 3rd order intercept point
- compression level
- desensitization level
- noise figure

Conversion loss and the intercept point are directly dependent upon the magnitude of the local-oscillator power. The prototype mixer's performance is offered in Figure 46, where the input intercept and conversion loss are plotted.

Both the compression and desensitization levels may appear to contradict reason. Heretofore, conventional diode-ring demodulators exhibited compression and desensitization levels an order of magnitude below the local-oscillator power level. However, with a commutation MOSFET mixer, switching is not accomplished by the injection of loop current but by the application of gate voltage. At a local-oscillator power level of + 17 dBm (50 mW), the 2-dB compression level and desensitization level were +30 dBm!

The single-sideband HF noise figure of 7.95 dB was measured at a local oscillator power level of +17dBm.

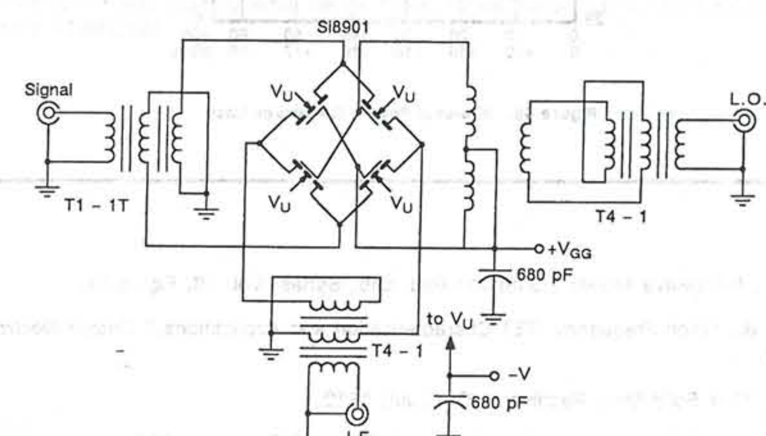

Figure 45. Prototype Commutation Double-Balanced Mixer

CONCLUSION

Achieving a high gate voltage to effect high-level switching by means of a resonant tank is not a handicap. Although one might, at first, label the mixer as narrow-band, in truth the mixer is wide-band. For the majority of applications, the intermediate frequency is fixed, that is, narrow band. Consequently, to receive a wide range of signal frequencies, the local oscillator is tuned across a similar band. In modern technology the tuning can be accomplished by numerous methods, not the least of which might be electronically using varactors. The resonant tank also may take several forms. It can be part of the oscillator, it can be varactor-tuned driver electronically tracking the local oscillator[21].

If the local-oscillator drive was processed to offer a more rectangular waveform, approaching the idealized square wave, we might then anticipate even greater dynamic range as predicted by Equation 37.

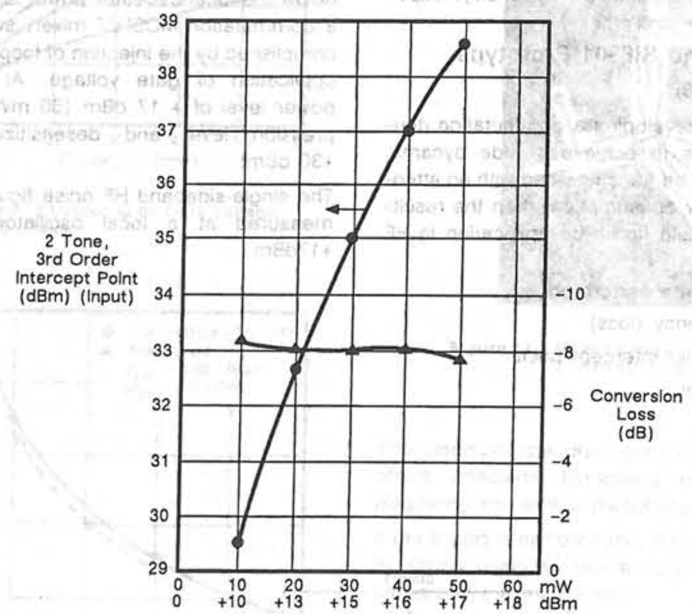

Figure 46. Intercept Point & Conversion Loss

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