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Try MOSPOWER™ FETs in your next Broadband Driver

August 1976

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INTRODUCTION

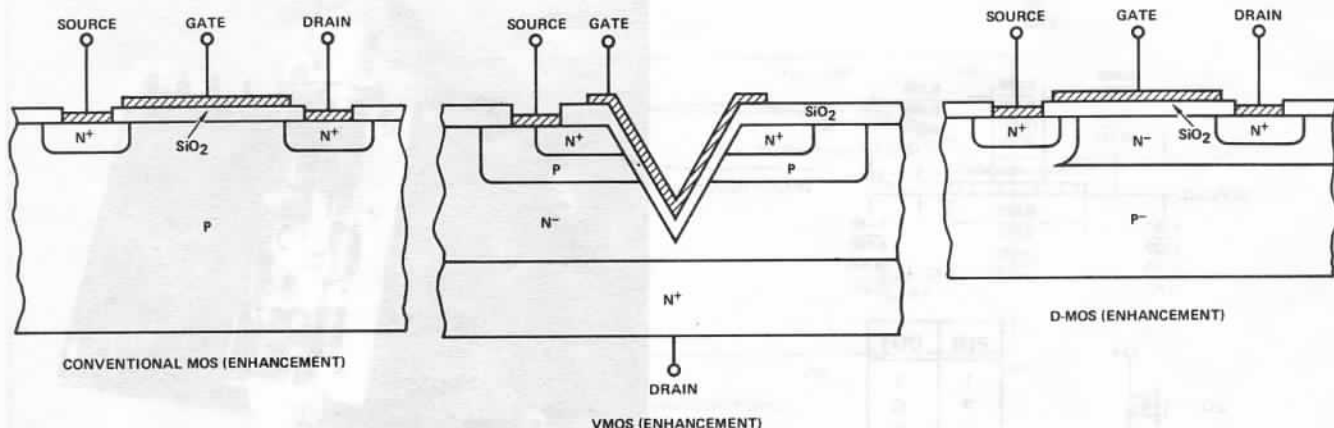
The MOSPOWER™ FET just introduced by Siliconix incorporated in 1976, is undoubtedly the most revolutionary semiconductor in decades and one that will open up exciting new applications heretofore impossible with bipolar transistors. Switching 1 ampere currents in less than 4 nanoseconds is commonly accomplished with this new power MOSFET. Among the many new features is one in particular that will interest those who seek for wide dynamic range: A linear transfer characteristic! Imagine, too, a transistor that can double for either a linear power amplifier or a wide dynamic range, low-noise, small-signal, front-end transistor!

Other features of the MOSPOWER FET are typical for field-effect transistors and especially desirable for power transistors. Like all FETs, there is no thermal runaway nor secondary breakdown, and no minority carrier storage time. The latter opens up interesting applications for class D (switching) amplifiers. Additionally, the MOSPOWER FET can accept any VSWR — open or short at any phase without any debilitating effects. Being an enhancement mode, N-Channel MOSFET one can operate in any class (A, AB, B or C) without needing negative power supplies for bias; zero bias providing class C service.

What is a 'MOSPOWER FET'?

Unlike the usual MOSFET which is 'planar' in construction, the MOSPOWER FET is a 4-layered vertical structure shown in comparison in Figure 1. This figure compares, somewhat oversimplified, the fundamental differences between MOS, DMOS and VMOS — which is the generic name for the MOSPOWER FET structure. Common to both MOS and DMOS (not VMOS) is the singular disadvantage which affects their power handling capabilities: The geometry requires massive area to handle the current necessary for power. A further disadvantage lies in their inability to accept high voltages. In the MOSPOWER FET, the current travels vertically, the source being on the top while the drain is the backside of the chip. In this vertical structure are 4 layers (N+/P/N-/N+) whose dimensions are precisely controlled by diffusion processes rather than by the less precision photolithographic methods common to the planar (MOS) technology.

VMOS offers high current densities, high source-to-drain breakdown capability and low gate-to-drain feedback capacity which makes the MOSPOWER FET a great power transistor for HF and VHF applications. Probably the most



Fundamental Differences in Enhancement-Mode MOS Structures
Figure 1

attractive aspect of this revolutionary semiconductor is its inherent linear transfer characteristic. In conventional MOS-FET (and JFET) this transfer characteristic is closely identifiable to a square-law response; that is, the drain current is proportional to the square of the gate-to-source voltage. However, in the VMOS structure the short channel causes the drain current to be linearly proportional to the gate-to-source voltage. Figure 2 provides a plot showing this effect.

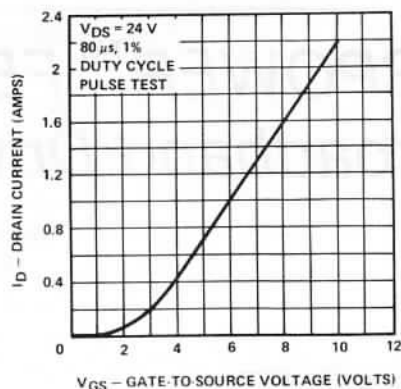


Figure 2

The MOSPOWER VHF FET: VMP 4

Packaged in the popular flange mount, 'opposing emitter' (in this case, opposing source) strip-line configuration (Figure 3) is the Siliconix VMP 4 capable of saturated output power approaching 20 watts at 160 MHz. The performance shown in Figure 4 represents the available *saturated* output power versus frequency when both the input and output impedances of the VMP 4 are conjugately matched, *not* in the circuit described in this article. Unlike the more widely used JFET (or MOSFET) the input and output impedances (in common source configuration) are particularly suited for

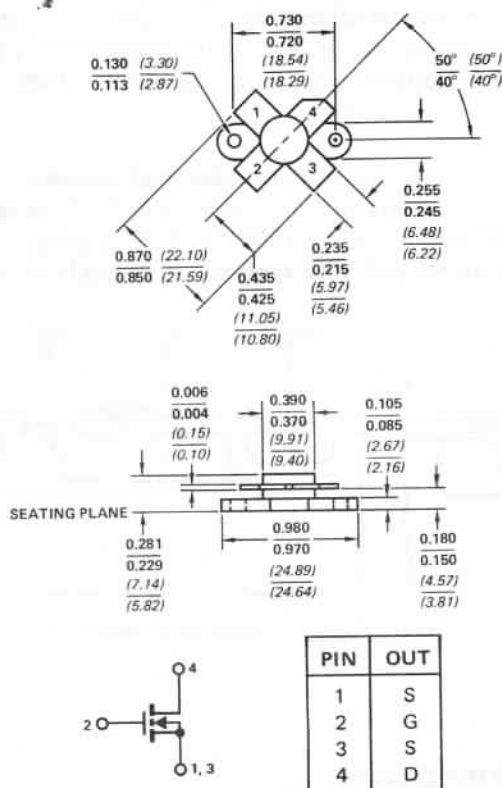


Figure 3

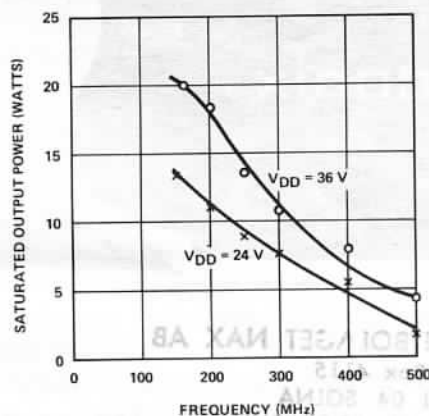


Figure 4

wideband amplifier service with *complete stability*. And very unlike power semiconductors these impedances are little affected by drive levels!

The Circuit

Simplicity is an understatement for this wideband power amplifier shown schematically in Figure 5 with a photo of the finished amplifier in Figure 6. Unlike many claims for broadband performance, this amplifier, by virtue of the negative feedback, performs with *flat* gain response (± 0.5 dB) over its entire operational bandwidth.

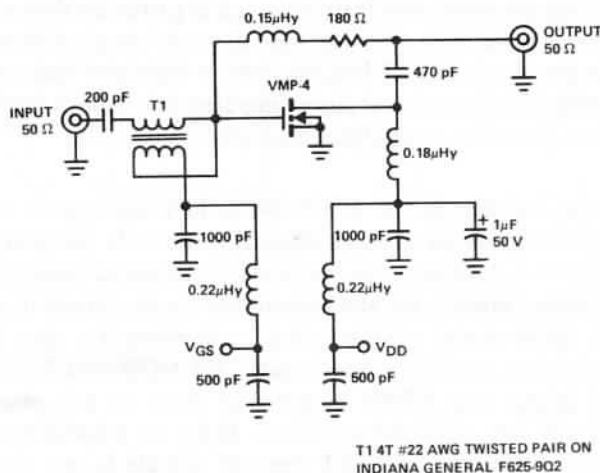


Figure 5

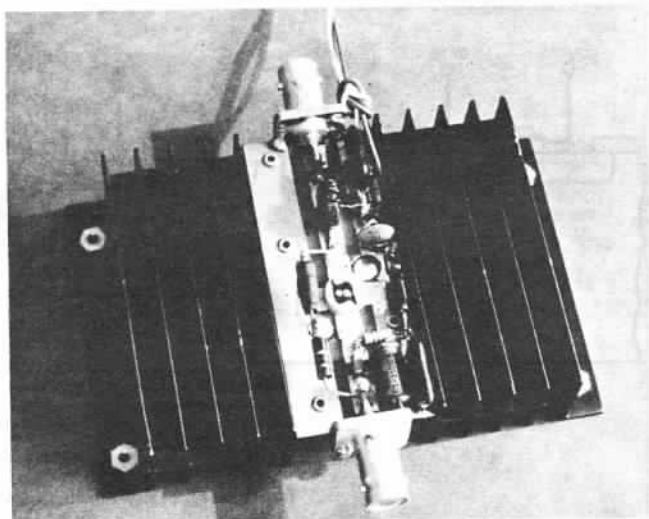


Figure 6

Two interesting features are immediately apparent in the circuit diagrams: 1) The simple 4:1 impedance balun for broadband input match; and, 2) Effectively no matching circuit on the output. My philosophy is, "Why use unnecessary parts if they're really not necessary?" To be sure, the drain circuit needs no further complication. Some may question the wisdom of such an almost over-simplistic design, especially in light of the familiar

$$R = \frac{(V_{CC} - V_{SAT})^2}{2P}$$

However, using this formula and making a few first-order assumptions, we can arrive at some near 50-ohm values of the drain load impedance; for example,

$$R = \frac{(25 - 3)^2}{2 \times 4} = 60.5 \text{ ohms}$$

To reach the lowest operational frequency requires a reasonably high permeability ferrite toroidal core, but in this design 6 meters was my low-end goal and the 220 MHz band uppermost, so an operational bandwidth extending from 40 MHz to 265 MHz was chosen.

Only one circuit trick was required to reach my upper frequency objective and in reality it wasn't so much a circuit trick as a careful component selection. The feedback inductor (0.15 μ Hy) cannot be one of those commercially available molded chokes — there appears to be too low a resonance, perhaps too much distributed capacitance. Wind your own. I used 6-8 turns of #30 AWG enamel on a 1/2 W 1 megohm resistor. If you have an inductance bridge you can set it exactly to 0.15 μ Hy, otherwise you may need to experiment. Using a molded choke will severely reduce your upper-frequency bandwidth.

Construction

About the only difficult aspect is preparing the double copper clad board to accept the flange mounted strip-line transistor. Careful layout and cutting will do a very acceptable job. As with any high-frequency layout, be sure to connect both copper clads (top and bottom) together either with small eyelets or what-have-you. Additionally, remember that

the MOSPOWER FET is MOS and has an unprotected gate, so don't handle it without first being absolutely sure that you are not carrying a static charge. Stay off rugs and out of crepe-sole shoes until you've got the transistor soldered into your circuit. Once in the circuit, you're free to do anything you want to with your amplifier.

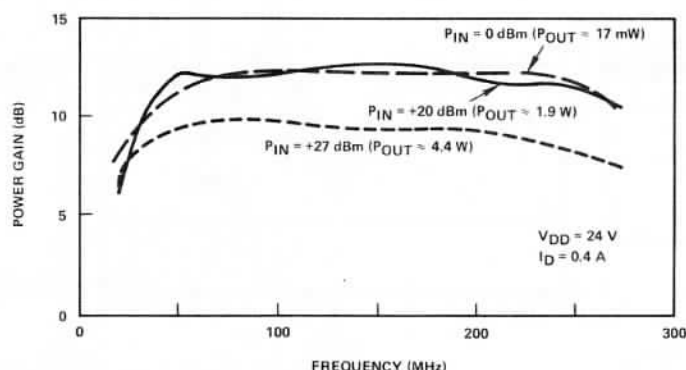
Since this transistor operates with healthy currents, it is absolutely necessary to mount the flange to a suitable heat sink. That pictured in Figure 6 is an overkill, but it does emphasize that a heat sink is necessary. Typical in any power heat sink one should use a suitable silicone grease or heat-sink compound.

A second precaution common to any high-current load is to watch out for small current-carrying molded chokes that may vaporize when the power is applied. I have found, quite by accident, that generally values of inductance *under* 0.22 μ Hy will hold up with currents of 1.5 A or less. Further proof of reliability in regard to this construction is that I have built 4 such identical amplifiers and all performed equally.

Performance

An interesting aspect of this wideband amplifier is that performance does not seem dependent upon whether one wishes to use it for a small-signal amplifier, say in the microwatt area of front-end receiver design, or for medium power (1-2 watts) amplification possibly to excite a linear final amplifier. Of special interest to those frustrated advocates of wideband amplifiers who are plagued by wideband noise problems will be the interesting fact that a MOSPOWER FET amplifier's wideband noise is literally unmeasurably low! For an example, this VMP 4 (any any other VMP device) offer excellent small-signal noise figures. A typical value of 2.4 dB at 146 MHz is easy to achieve with a properly matched input circuit. Now, not to be misunderstood, this particular circuit using the 4:1 balun is *not* properly matched for optimum small signal noise figure. But that was not the original objective in the first place.

Bandwidth for two power levels is shown in Figure 7. I'm sure that what variations there are were entirely caused by measurement procedures. With a 1 dB compression occurring



Power Gain Bandwidth
Figure 7

at an input level of +23 dBm, the +27 dBm input level is understandably under compression; hence the lower gain figure.

Two tone, 3rd order, intermodulation performance measured at both 100 mW and at 1 watt output levels is displayed in Figure 9 as Intercept Point. Intercept Point was calculated referenced to a single tone output using the formula:

$$\text{I.P. (dB)} = P_{\text{OUT}} (\text{dB}) + \frac{P_{\text{IMD}} (\text{dB})}{2}$$

When calculating Intercept Point, or more truthfully, when *comparing* with values of advertised products, great care must be taken to know exactly how the specification was

arrived at. To 'improve' your figure some may reference the PEP output (see Figure 8) or even the average power output. Figure 9 offers the most conservative — referencing the single tone.

In conclusion remember, this MOSPOWER FET is not sensitive to load mismatch, so during your testing feel free to disconnect your load without removing the drive power. If you feel compelled to tweak with screwdriver or capacitor, again there is no problem should you short your power supply buss. Sparks may fly but when the smoke clears, your FET will still be ready for action. In retrospect, power MOSFETs appear to have three fundamental advantages: 1) very easy to match; 2) extremely rugged; and 3) can be paralleled without fear of disastrous consequences.

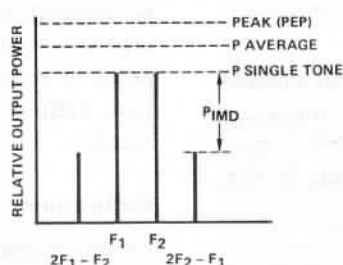


Figure 8

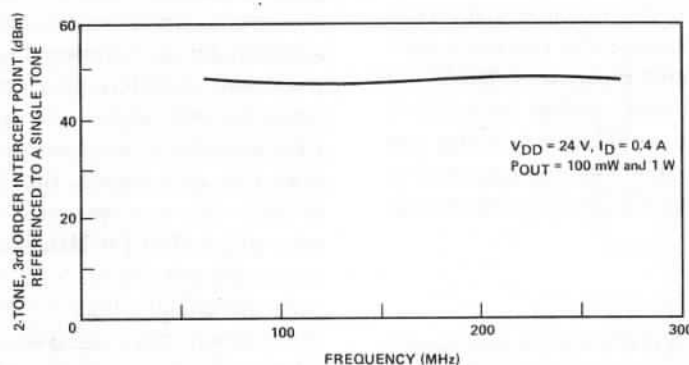


Figure 9

Siliconix assumes no responsibility for circuits shown, nor does it represent or warrant that they do not infringe any patents.

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