APPLICATION NOTE

FETs in Balanced Mixers

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INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than

Table I

Characteristic	MIXER TYPE Single-Ended	 Single Balanced	 Double Balanced
Bandwidth	Several decades possible	Decade	Decade
Relative IM Density	1.0	0.5	0.25
Interport Isolation	Little	10-20 dB	>30 dB
Relative L.O. Power	0 dB	+3 dB	+6 dB

Table II

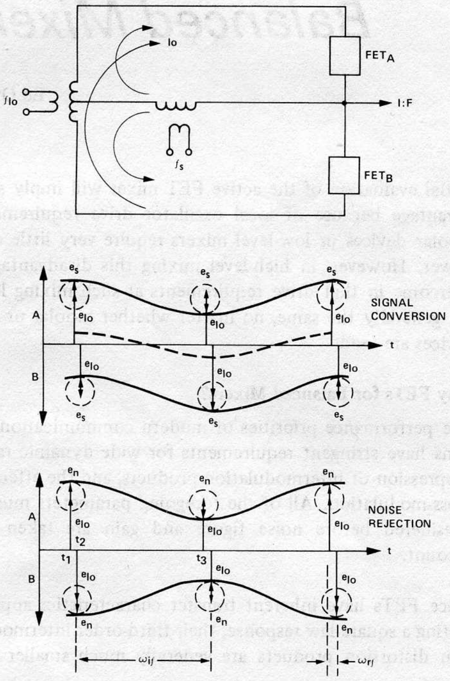
DEVICE	ADVANTAGES	DISADVANTAGES
Bipolar Transistor	Low Noise Figure High Gain Low D.C. Power	High IM Easy Overload Subject to Burnout
Diode	Low Noise Figure High Power Handling High Burn-out Level	High L.O. Drive Interface to I.F. Conversion Loss
JFET	Low Noise Figure Conversion Gain Excellent IM products Square Law Characteristic Excellent Overload High Burn-out Level	Optimum Conversion Gain not possible at Optimum Square Law Response Level High L.O. Power
Dual-Gate MOS FET	Low IM Distortion AGC Square Law Characteristic	High Noise Figure Poor Burnout Level Unstable

those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).



Signal and Noise Vectors
Figure 1

Energy conversion into the intermediate frequency (IF) passband is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate (ω_{ift}); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time (t_1) the noise component (e_n) is "in phase" with the local oscillator vector (e_{1o}) and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time t_2, the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced 180° (ω_{ift}) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise.(1)

The analysis of the conversion of the signal to the IF passband is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time t_2, the signal vector (e_s) is "out of phase" with the local oscillator vector, e_{lo}. The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a *prototype* balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

(1) Intermodulation and Cross-Modulation
(2) Conversion Gain
(3) Noise Figure
(4) Selecting the Proper FET
(5) Local Oscillator Injection
(6) Designing the Input Transformer
(7) Designing the IF Network

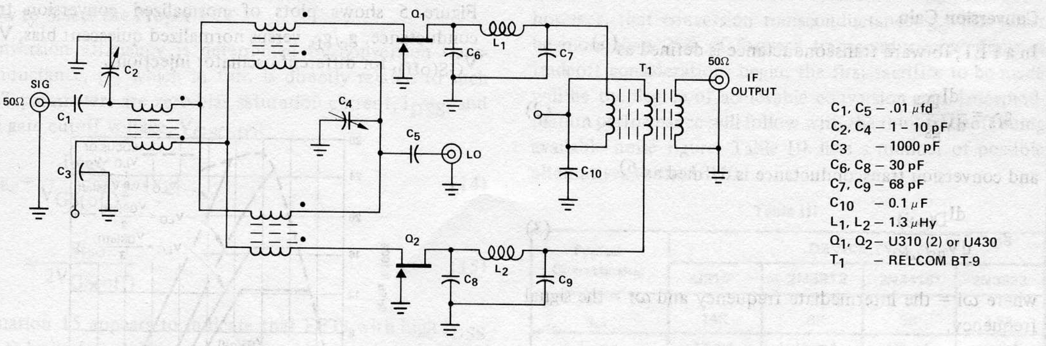
Intermodulation and Cross-Modulation

A basic aim in mixer design is to avoid the effects of intermodulation product distortion and crossmodulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both crossmodulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest.(2)

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an N-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance, g_c, is achieved at about 80% of the FET gate cutoff voltage, $V_{GS(off)}$, and amounts to about 25% of the forward transconductance, g_{fs}, of the FET when used as an amplifier.



Prototype Active Balanced Mixer
Figure 2

Since conversion gain (or loss) must be considered, it is common to equate voltage gain A_V, as:

$$A_V = g_c R_L \tag{1}$$

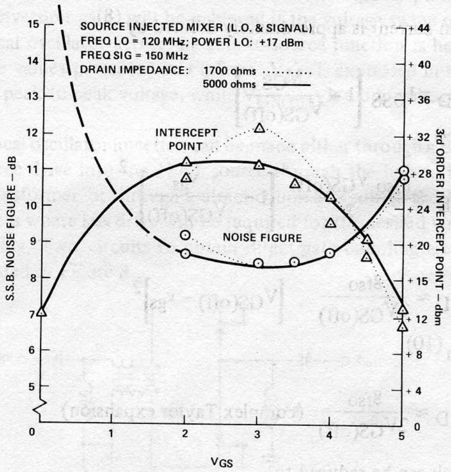
where g_c is the conversion transconductance and R_L is the FET drain load.

An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion – particularly intermodulation product distortion.

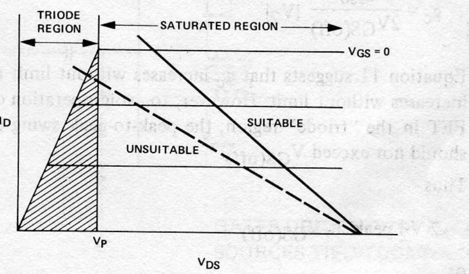
Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called "varactor effect."

The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted crossmodulation signals.[3] A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated ("triode") region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 18 through 20.

Distortion from the "varactor effect" is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-sorce voltage can cause a change in parasitic capacitance, C_{rss}, and give rise to harmonics.[4] A FET tends to be voltage-dependent when the drain voltage falls appreciably below 6 volts. If the source voltage (from the power supply) is also low and the drain load impedance is high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.



Comparison of Mixer IM Characteristics
Figure 3



Plotting Drain Load Lines
Figure 4

Conversion Gain

In a FET, forward transconductance is defined as[5]

$$g_{fs} = \frac{dI_D}{dV_{gs}} \tag{2}$$

and conversion transconductance is defined as[6]

$$g_c = \frac{dI_D(\omega i)}{dV_{gs}(\omega r)} \tag{3}$$

where ωi = the intermediate frequency and ωr = the signal frequency.

The effects of time-varying local oscillator voltage, V_2, and the much smaller signal voltage, V_1, must be considered:

$$v_{gs} = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \tag{4}$$

For square law operation[7]

$$V_2 + V_{GS} \leqslant V_{GS(off)} \tag{5}$$

Drain current is approximately defined by[8]

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \tag{6}$$

or[9]

$$I_D \approx \frac{g_{fso}\, V_{GS(off)}}{2}\left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \tag{7}$$

or

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}}\left[V_{GS(off)} - v_{gs}\right]^2 \tag{8}$$

then[10]

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \quad \text{(complex Taylor expansion)} \tag{9}$$

which can be reduced to

$$I_{D(IF)} \approx \frac{g_{fso}}{2V_{GS(off)}}\, V_1\, V_2 \cos(\omega_1 - \omega_2)t \tag{10}$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2V_{GS(off)}}\, |V_2| \tag{11}$$

Equation 11 suggests that g_c increases without limit as V_2 increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of V_2 should not exceed $V_{GS(off)}$.

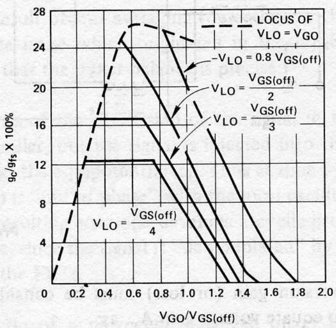
Thus

$$2\,V_2 \text{ peak} \leqslant V_{GS(off)} \tag{12}$$

or

$$V_2 \text{ peak} \leqslant \frac{V_{GS(off)}}{2} \tag{13}$$

Figure 5 shows plots of normalized conversion transconductance, g_c/g_{fs} versus normalized quiescent bias, $V_{GS}/V_{GS(off)}$, for different oscillator injections.

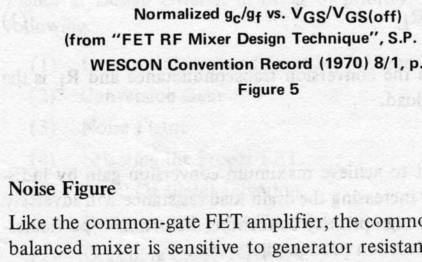


Normalized g_c/g_f vs. $V_{GS}/V_{GS(off)}$
(from "FET RF Mixer Design Technique", S.P. Kwok, WESCON Convention Record (1970) 8/1, p.2.)
Figure 5

Noise Figure

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance, R_g.[11] A change of a decade in R_g can produce a noise figure variation of as much as 3 dB.

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance, g_{igs}, which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.



Power Gain and Noise Matching
Figure 6

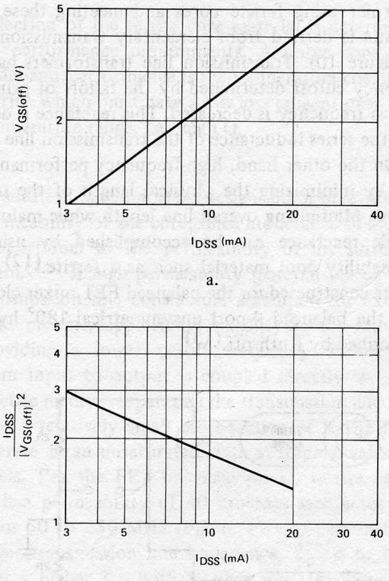
How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance, g_c, which in turn is directly related to such FET parameters are zero-bias saturation current, I_{DSS}, and the gate cutoff voltage, $V_{GS(off)}$:

$$g_c = \frac{I_{DSS}}{V_{GS(off)}^2} |V_2| \tag{14}$$

$$\approx \frac{g_{fso}}{2V_{GS(off)}} \tag{15}$$

Equation 15 appears to indicate that FETs with high I_{DSS} are to be preferred. However, I_{DSS} and $V_{GS(off)}$ are related, and Figures 7A and 7B show that devices from a family selected for high I_{DSS} do *not* provide high conversion transconductance, but actually produce a lower value of g_c.



Relationship of I_{DSS} and $V_{GS(off)}$
Figure 7

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS}, for dynamic range. A match to 10% is generally adequate. Among currently available devices; the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 20,000 μmhos max at V_{DS} = 10 V, I_D = 10 mA, and f = 1 kHz.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach – the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310. Remember, however, that conversion transconductance, g_c, can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure. Table III lists a number of possible alternatives to the U310.

Table III

Typical Characteristic	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	14K	6K	5K	3.5K
I_{DSS}	40 mA	15 mA	10 mA	10 mA

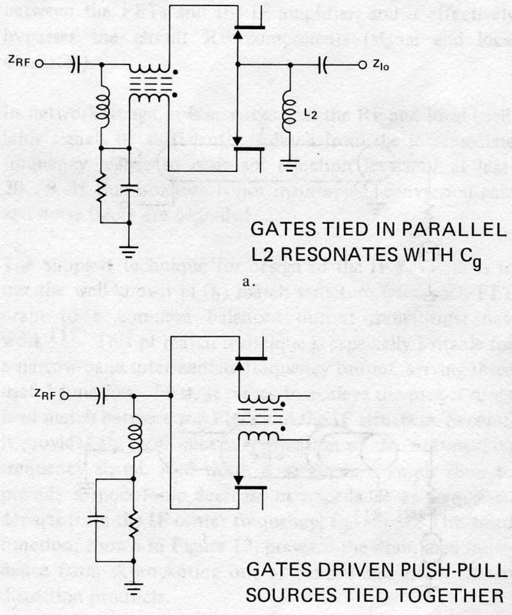
*Similar devices are also available in plastic packages:

U310 (J310)
2N4416 (2N5486, J304-18)

Local Oscillator Injection

Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5. V_{LO} is expressed in terms of peak-to-peak voltage, while $V_{GS(off)}$ is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing, Two circuits to obtain direct gate coupling are suggested in Figure 8.



Alternate Forms of L.O. Injection
Figure 8

The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer. best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-ohm load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

Designing the Input Transformer

Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

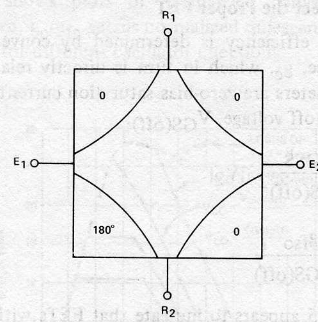
(1) Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B

(2) Offer a match between either input to a symmetrical balanced load

(3) Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)

(4) Maintain a differential phase of 180° across the symmetrical balanced loads

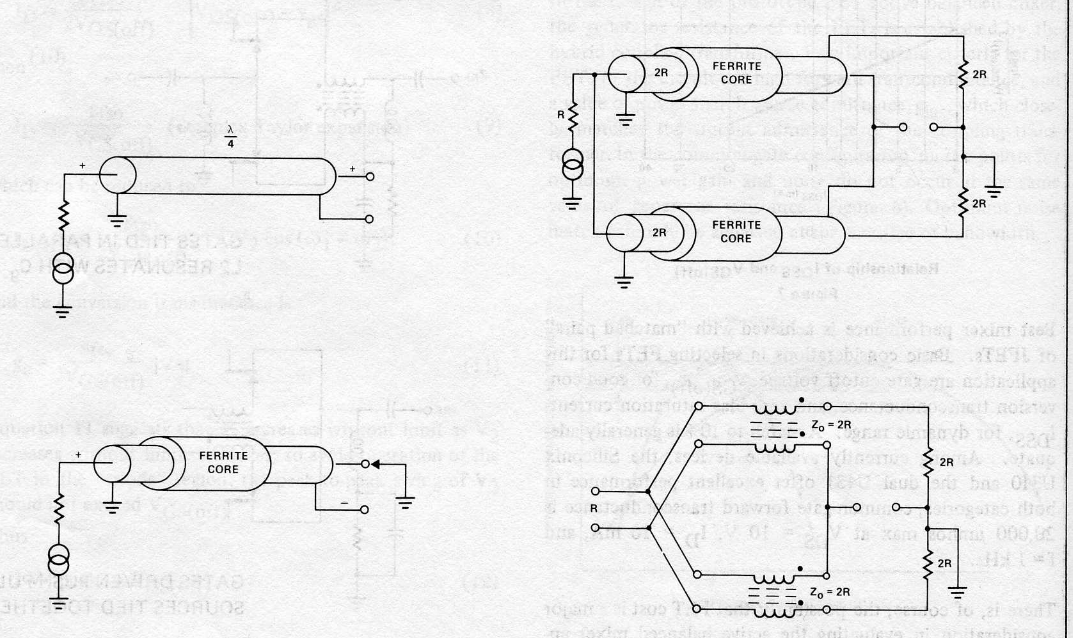
(5) Introduce the least possible amount of loss



4-Port Hybrid with Phase and Isolation

Figure 9

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite.(12) The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff.(13)



Hybrid Input Coupling Transformer

Figure 10

Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis.[14] The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{upper}} \text{ (inches)} \tag{16}$$

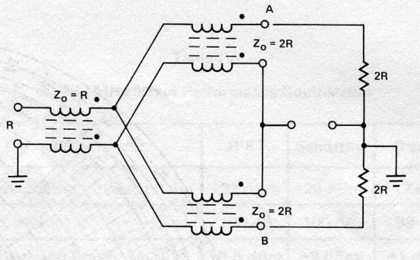
$$\text{min length} = \frac{20\, R_L}{(1 + \mu/\mu_o)\, f_{lower}} \text{ (inches)} \tag{17}$$

where R_L = the load impedance, μ/μ_o = the relative permeability of the ferrite at the lower frequency, and n = a fractional wavelength determined by the amount of allowable phase error.

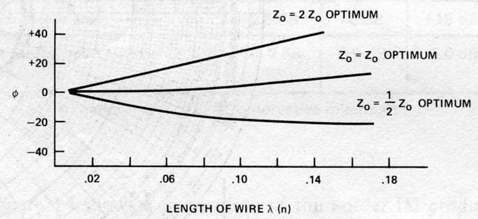
Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high Q.

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium.[15] A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line condcutors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance, Z_o, is to be preferred over a higher Z_o. Both 50-ohm and 100-ohm transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45 Ω is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while 3½ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide Z_o = 100 ohms. Each core is wound with 2 inches of the proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 16, 17).

As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated (C_2, C_4, Figure 2).[16] A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within ±2 degrees (about 180°) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) – but phase track beyond 250 MHz *may* show too much deterioration.



a.



b.

Toroid Coil Winding Data
Figure 11

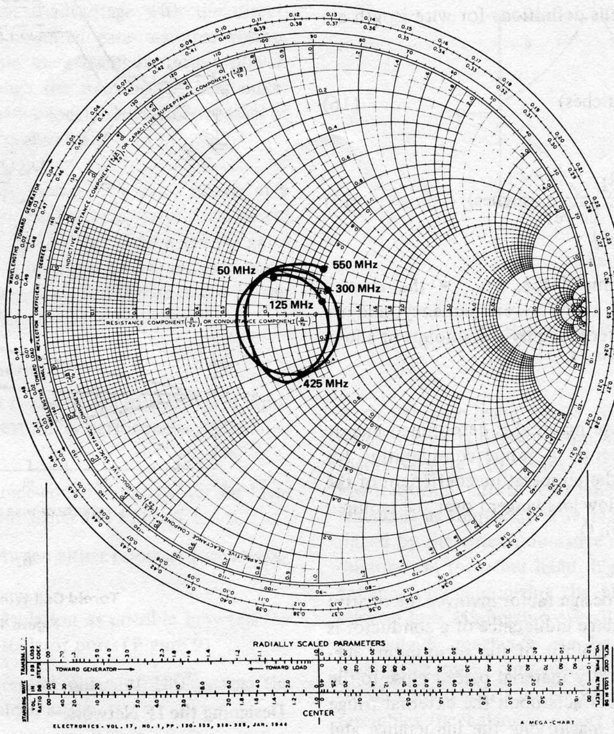
Designing the IF Network

The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi (π) match structure from each FET drain to a common balanced output transformer network.[17] This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency, f_o.[18, 19] This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and crossmodulation will be



50Ω – 200Ω Balun

Figure 12

both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors.[20] If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2\,V_{GS(off)}}{i_d} \tag{18}$$

where

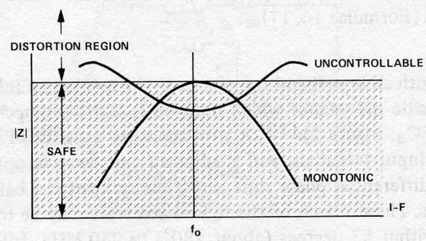
$$i_d = I_{DSS}\left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \tag{19}$$

and

$$v_{gs} = V_{GS} + V_1 \sin \omega_1 t \tag{20}$$

For the U310 FET, the optimum drain load impedance is established at slightly less than 2000 ohms, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-ohm CT to 50-ohm trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 ohms on each FET; excellent



Pi (π) Match Filter Function

Figure 13

IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

Mixer Performance

Tests of the operational prototype FET balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table IV (measurements of all three mixers were made under laboratory conditions).

Table IV

50-250 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dBm	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8.5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+2.5 dB*	−6 dB	+18 dB
Single-sideband Noise Figure @ 50 MHz	7.2 dB	6.5 dB	6.0 dB

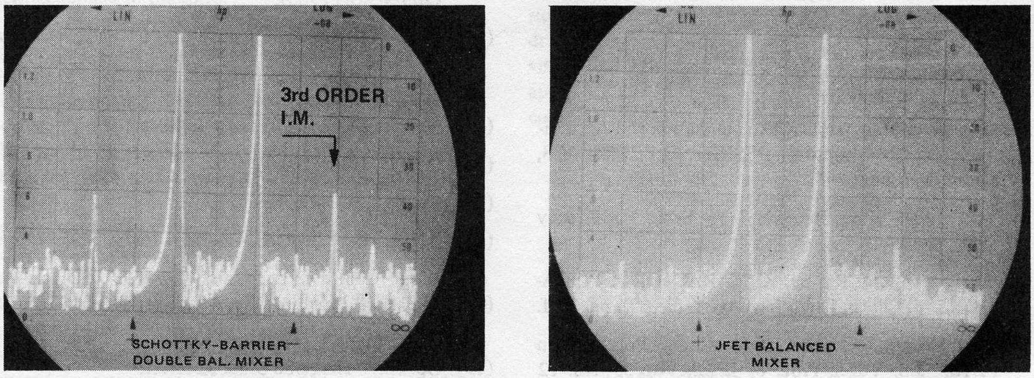
†Estimated *Conservative minimum

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point.[21] With two signals 300 kHz apart, the balanced mixer suppressed third-order products −89 dB with both signals at −10 dBm, representing an intercept point of +32 dBm.

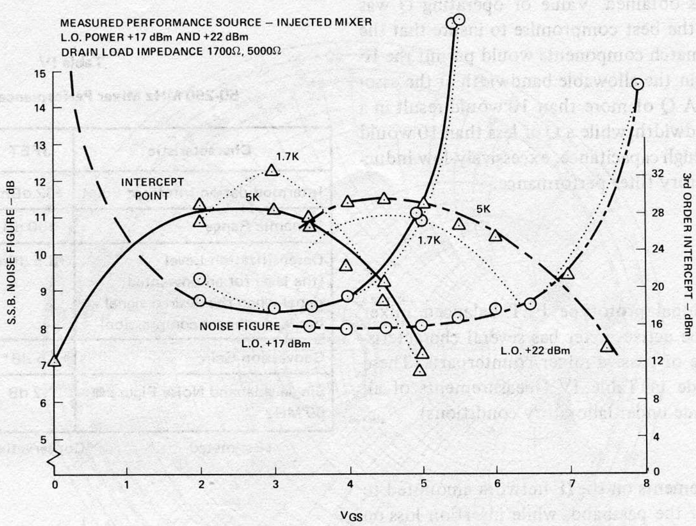
Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.



Comparison of 3rd Order IM Products

Figure 14



Noise Figure and Intercept Point Performance

Figure 15

CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 16 and 17) are equally applicable to trifilar as they are for bifilar.

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(12) O. Pitzalis and T. Couse, "Broadband Transformer Design for RF Transistor Power Amplifiers," ECOM-2989, July 1968. Also in **Proc. Electronic Component Conference** (1968).

(13) "Some Broadband Transformers," C.L. Ruthroff, **Proc. IRE**, Vol. 47, Aug. 1969, pp. 1337-1342 (Figure 7(b).

(14) Op. cit., ECOM-2989, July 1968.

(15) Op. cit., ECOM 2989, p. 6.

(16) Op. cit., ECOM 2989, p. 7.

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(18) "Reactive Loads – The Big Mixer Menace," P. Will, MICROWAVES, April 1971, pp. 38-42.

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